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\* CLARIFICATION TO THIS NOTICE \*  
\* OF 4/15/84 \*  
\* SEE NOTE BELOW \*  
\*\*\*\*\*

Title: APPLE /// PROFILE INTERFACE CARDS

PROBLEM

Potential problems in random data handling/command errors may arise with Apple /// and Profiles when the new RFI shielded cables are used with earlier versions of the Apple /// interface card. End Users may get a large number of "Bad Block" indications and in some instances, the Profile is unable to read files saved and sector damage is indicated.

CAUSE

Resistor Array values on the Apple /// Interface Card (at location DM 1 and DM 2) were changed from 330 Ohms to 100 Ohms. Interface Cards with the 330 Ohms resistor arrays (manufactured prior to October 1983) are not compatible with the new Profile Shielded Cable, P/N 590-0202. When the older interface cards are connected to the shielded cables, an impedance mismatch occurs that results in error messages.

ACTION

- The flat ribbon cables (P/N 590-0046) will operate on either the 330 Ohm or the 100 Ohm revisions Interface Card.
- If the RFI Shielded Cable (P/N 590-0202) is to be used, the Apple /// Interface Card for the Profile must have 100 Ohm resistor Arrays at location DM 1 and DM 2. The 100 Ohm resistor Arrays (P/N 112-0001) replace the old 330 Ohm resistor arrays.
- It is recommended that the Apple /// Interface Cards in the Profile Accessory Kits be checked for the 100 Ohm resistor arrays before sale to an end user.

NOTE: 10/15/84 Clarification

WHERE 100 OHM IS MENTIONED ABOVE, THE ACTUAL TERM SHOULD BE  
8 X 100 OHM DIP

APPLE COMPUTER, INC  
INTERNATIONAL SERVICE  
LEVEL II SERVICE MANUAL UPDATE  
PRODUCT: ProFile, 072-0116

UPDATE #1  
10/12/84

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Bills of Materials A9M1005
Bills of Materials A3M0305

PEN & INK CHANGES

<u>PAGE NUMBERS</u>	<u>CHANGE ACTIONS</u>
1 (How to Use This Manual)	Delete "Page i" at bottom center of page.
Pages 3.3 thru 3.9	Change "Appendices" at bottom left of pages to read "Appendix A".
Pages 3.10 thru 3.19	Change "Appendices" at bottom left of pages to read "Appendix B".
Pages 3.20 thru 3.26	Change "Appendices" at bottom left of pages to read "Appendix C".
Pages 3.27 thru 3.123	Change "Appendices" at bottom left of pages to read "Appendix D".
Schematics	Write "Appendix E" at bottom left of all schematics pages.

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**Please list any technical errors found in this manual on a sheet of paper and attach it to a copy of this form. Be sure to include the page and paragraph of the error, and to provide a correction.**

**If you feel that any information needs to be clarified, added, or explained in greater detail, or if you think that the manual could be laid out in a better order or format, please note that on a sheet of paper and return it also. Include the page and paragraph to be expanded, or a description of the missing information, or a description of the job you are performing for which more detail is required, or your suggested format/layout.**

**Though we would like to get these forms back with written feedback, E-mail or Telex responses will be gratefully accepted.**

**Remember, your feedback will help to ensure that this manual gets corrected and improved, and that future revisions and manuals may more fully meet your needs.**

**Manual: PROFILE, 072-0116**

**Reviewer's Name: \_\_\_\_\_ Date: \_\_\_\_\_**

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AFER Service, Technical Support  
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## **HOW TO USE THIS MANUAL**

The Pro-File Phase 1 Service Manual is divided into 3 sections:

### **SECTION 1 TROUBLESHOOTING:**

This section contains a flowchart procedure and corresponding explanation for troubleshooting a problem Pro-File to the faulty module.

### **SECTION 2 SERVICE PROCEDURES:**

This section contains the various procedures needed to test, adjust, and remove or replace the modules on the Pro-File.

### **SECTION 3 APPENDICES:**

This section contains various descriptions referred to by the other sections for the purpose of providing general and specific information on Pro-File operation.

PROFILE EQUIPMENT LIST

- 1) DEBUGGER:
  - FIRMWARE.....889-9007
  - Z8.....338-8603
  
- 2) SOFTWARE DUPLICATION:
  - FST.....889-0029
  - QUICK DEBUG (Ver. 7).....889-0004
  - FORMAT CERTIFY.....889-0013
  - BIG DEBUG (Ver. 17).....(INCLUDED)
  
- 3) UPGRADE KIT:
  - MASKED Z8 MICROPROCESSOR.....341-0171
  - 6.36 x 5/16 STANDOFF.....860-0213
  - 5.1K OHM RESISTER.....101-4512
  - 0.1 MICROFARAD CAPACITOR.....130-0007
  - 1K OHM RESISTER.....101-4102
  - 330 OHM DIP PACKS.....112-0105
  - 3.9K OHM RESISTER.....101-4392
  - 26 TO 30 GAUGE INSULATED WIRE.....N/A
  
- 4) MISCELLANEOUS TOOLS:
  - TEST LED.....590-0047
  - (CUT DOWN)
  - JUMPER
  - (USED DURING FORMAT)
  - ALLEN (hex) DRIVERS
  - (BRAKE ADJUSTMENT 5/64)
  - (TRACK ADJUSTMENT .050)

**Material Requirements  
For Repair of  
5MB ProFile**

Known Good Test Unit:

A9M0005/A9M1005 ProFile System, 115V/230V

Documentation :

072-0116 ProFile Level II Service Manual  
204-1011 Level II Technical Reference (Schematics)  
Volumes I, II & III

Diskettes :

077-0010 A3/ProFile Diagnostic Diskette  
077-0039 Limited Data Recovery  
889-0004 Quick Debug Diskette  
889-0013 Format/Certify Diskette  
889-0029 Final System Test Diskette  
XXX-XXXX D-Bug Diskette

Tools/Tooling/Supplies :

Apple /// System  
A3M0001 Silentype Printer  
5/64" Allen (Hex) Driver  
.050" Allen (Hex) Driver  
.010" Wire Gauge  
.070" Wire Gauge  
.010" Flat Gauge  
.030" Flat Gauge

Hardware:

101-4102 Resistor, 1K ohms 5%  
101-4512 Resistor, 5.1K ohms  
112-0105 Resistor Array, 330 ohms DIP  
112-0107 Resistor Array, 100 ohms DIP  
130-0007 Capacitor, 0.1uf  
338-8603 Z8 Firmware  
341-0171 IC, Masked Z8 Microprocessor  
590-0047 Test LED  
860-0213 6.36 x 5/16 Standoff  
889-9007 IC, EPROM Debugger Firmware



## Level II Repair Center Common Material Requirements

1. **TEST EQUIPMENT:**
  - Dual Trace Oscilloscope
  - High Voltage Probe
  - HTR1005B-S Huntron Tracker
  - HSR410 40-Pin Huntron Switcher
  - Digital Multimeter
  - Frequency Counter
  - Continuity Tester
  - 890-8011 115V Z5212 Power Supply Tester
  - 890-7030 Z5212 A2 Load Module
  - 890-7031 Z5212 A3 Load Module
  - 890-7032 Z5212 ProFile Load Module
2. **DOCUMENTATION:**
  - 204-1011 Level II Technical References (Vol's I, II & III)
3. **TOOLS/TOOLING/SUPPLIES:**
  - 916-0001 Circuit Cooler
  - 918-0003 Solder SN60/20S.W.G.
  - 918-0017 IC Puller
  - Solder Station
  - Solder Remover
  - Flux Solvent and Acid Brush
  - Heat Gun
  - Set of Slotted Screwdrivers
  - Set of Phillips Screwdrivers
  - Set of Jeweler's Screwdrivers
  - Magnetic Screw Retriever
  - Set of Hex (Allen) Wrenches
  - Needle Nose Pliers
  - Duck Bill Pliers
  - Wire Cutters
  - Diagonal Cutters
  - Wire Strippers
  - X-acto Knife
  - Scribe
  - Magnifying Glass with Light
  - Industrial Grade Alcohol (90% or better)
  - IC Clips, 16, 20, 24, and 40 Pins
  - 26 gauge green wire
  - 12-inch Jumper Wire with Insulated Clips
  - Jumper Leads
  - Heat Sink Hemostats
  - Safety goggles
  - Heavy Duty Vise (for power supplies)
  - PCB Vise (for desoldering/soldering PCB's)
  - Desk Top Storage Container for Hardware
  - Anti-static Foam Pads 12x18 inches
  - Reversible Drill and Bits
  - Small Sonic Cleaning Tank
  - Mirror for Monitor Repairs
  - Hammer
  - Punch for knocking pop rivets out of power supplies
  - Large Roll-around Racks
  - Small Roll-around Racks
  - Shelving for Material Awaiting Repair
4. **HARDWARE:**
  - 590-0003 115V AC Power Cord

**ProFile  
Phase 1 Service Manual**

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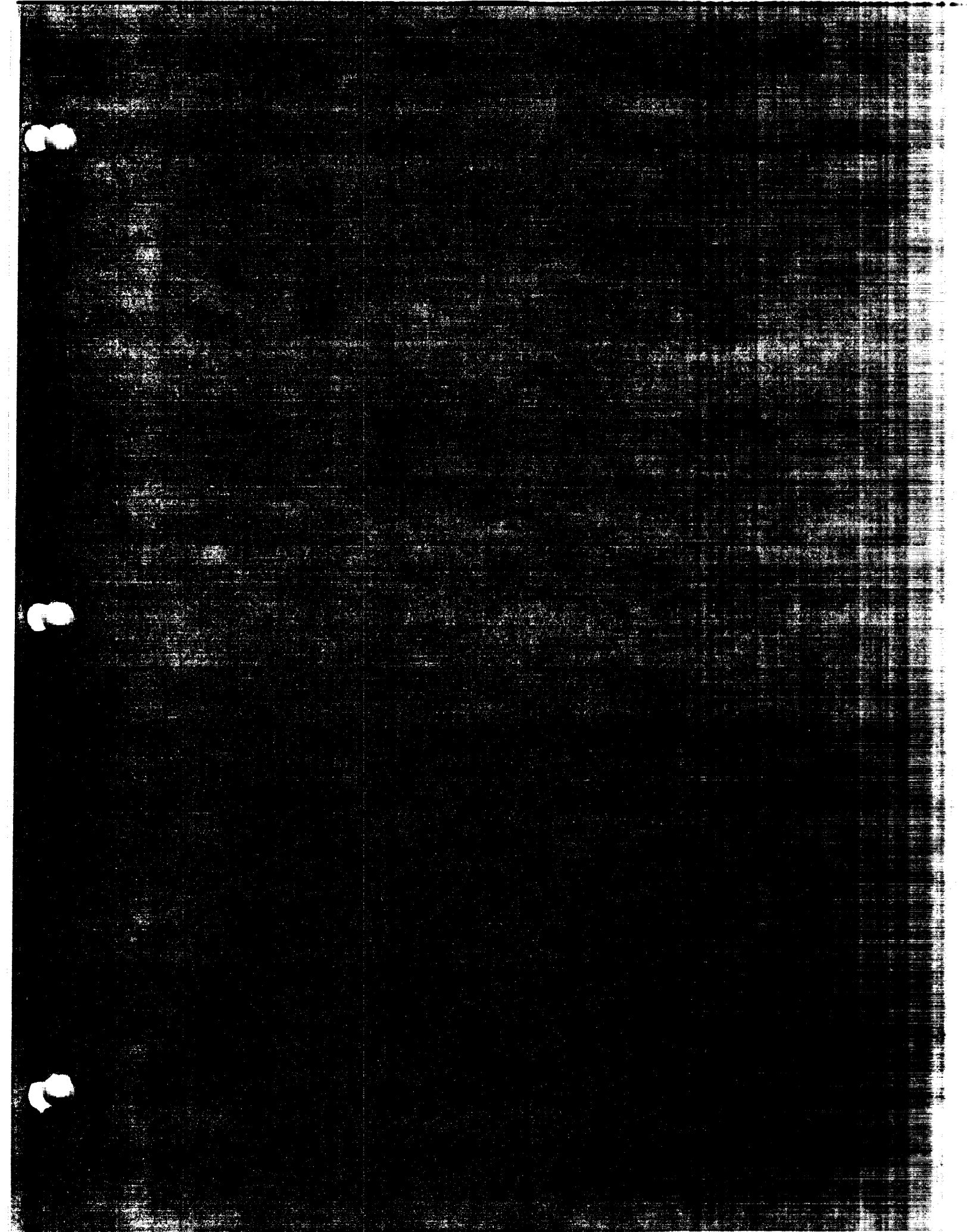
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050-4034, Controller Lisa 2.0	
050-5005, Analog	
050-5025, I/O Board (ProFile/Apple ///)	
050-5007, Apple /// Interface	
050-5009, 120V/240V Switchable Power Supply	
Bills of Materials -----	Appendix F
661-92049, Controller	
661-92048, Analog	
661-92050, Interface Card	
A9M0005, U.S. Generic ProFile	
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**SECTION 1**  
**TROUBLESHOOTING**

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## IMPORTANT READ THIS

### HOW TO USE THIS SECTION

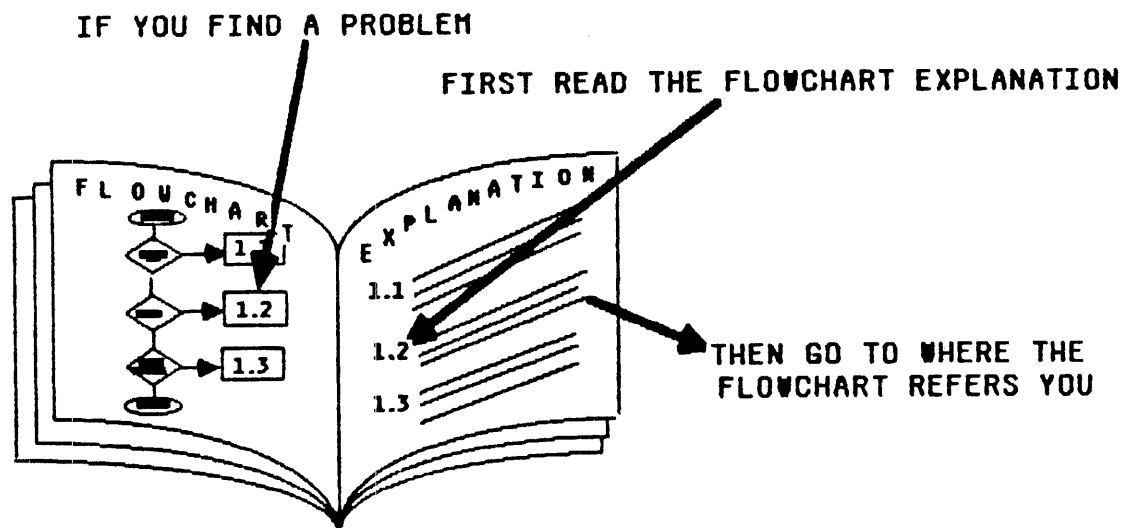
The procedure in this Troubleshooting Section is concerned with isolating a problem in the Pro-File to a malfunctioning module (i.e. Controller PCB, Analog PCB, Hard Disk Assembly (HDA), or Power Supply).

**CAUTION:** The Hard Disk Assembly (HDA) is a very expensive and fragile device, handle it gently to avoid damage.

To troubleshoot the Pro-File use the flowcharts in this section beginning with the main flowchart on the next page.

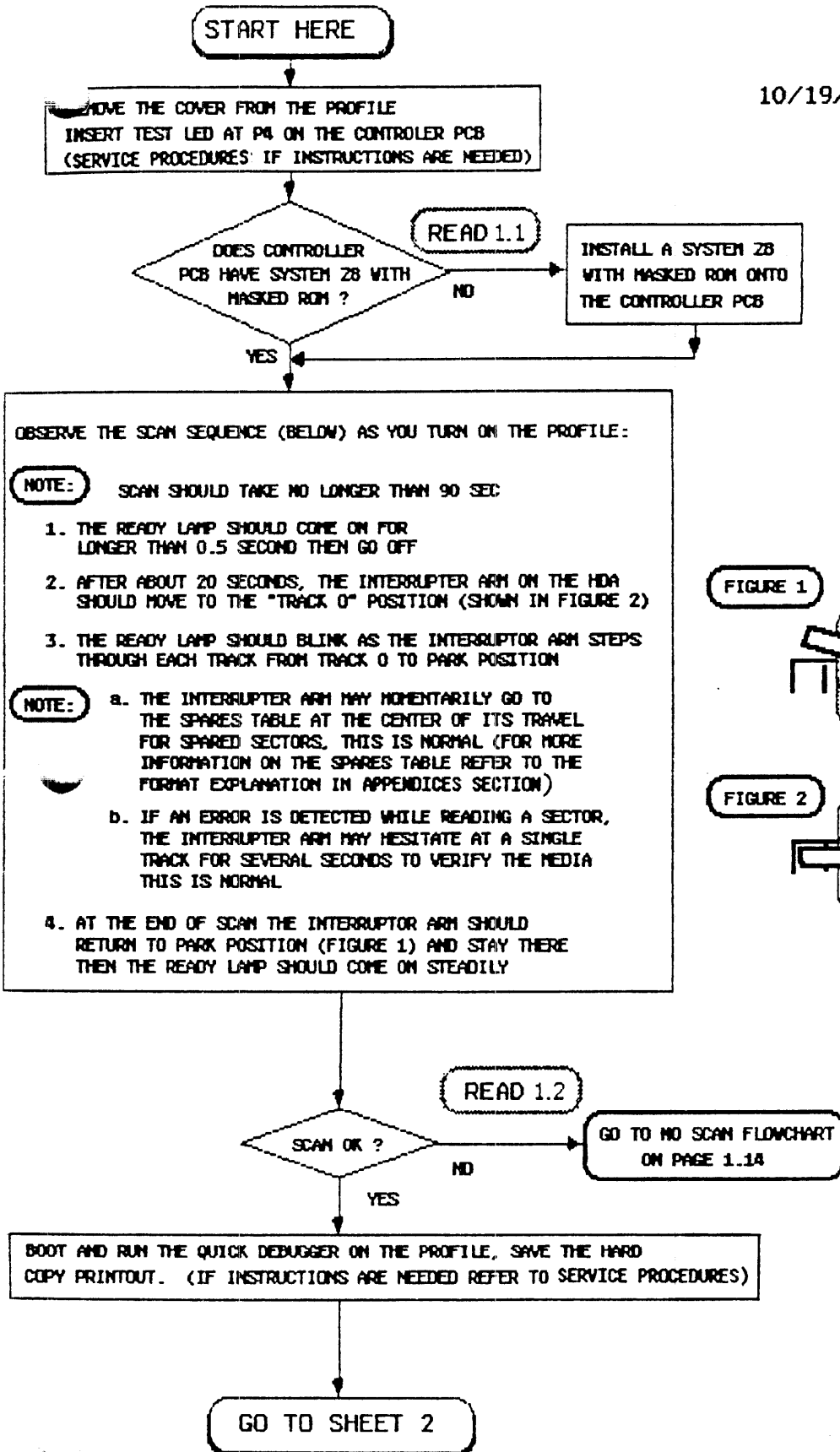
If you find a problem, go to the opposite page and read the explanation for the check that failed. This explanation will provide you with valuable information on the reasoning behind the flowchart, and will also provide you with references to sections 2 and 3 for needed procedures and additional information. After reading the flowchart explanation, you may if you wish take the action indicated at the NO branch of that check.

\* If you are not familiar with Pro-File operation you may wish to read the Pro-File HDA description and/or the Pro-File Overview in the Appendices Section.





10/19/83



OBSERVE THE SCAN SEQUENCE (BELOW) AS YOU TURN ON THE PROFILE:

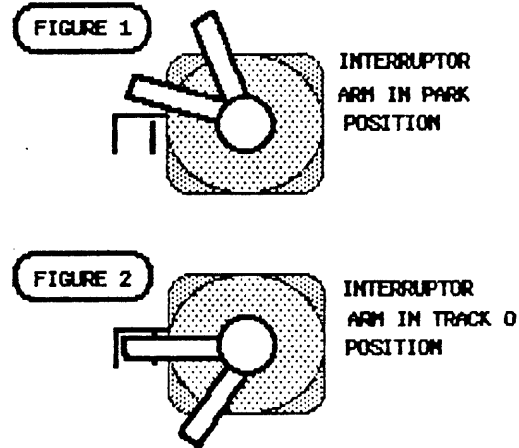
**NOTE:** SCAN SHOULD TAKE NO LONGER THAN 90 SEC

1. THE READY LAMP SHOULD COME ON FOR LONGER THAN 0.5 SECOND THEN GO OFF
2. AFTER ABOUT 20 SECONDS, THE INTERRUPTER ARM ON THE HDA SHOULD MOVE TO THE "TRACK 0" POSITION (SHOWN IN FIGURE 2)
3. THE READY LAMP SHOULD BLINK AS THE INTERRUPTER ARM STEPS THROUGH EACH TRACK FROM TRACK 0 TO PARK POSITION

**NOTE:** a. THE INTERRUPTER ARM MAY MOMENTARILY GO TO THE SPARES TABLE AT THE CENTER OF ITS TRAVEL FOR SPARED SECTORS. THIS IS NORMAL (FOR MORE INFORMATION ON THE SPARES TABLE REFER TO THE FORMAT EXPLANATION IN APPENDICES SECTION)

d. IF AN ERROR IS DETECTED WHILE READING A SECTOR, THE INTERRUPTER ARM MAY HESITATE AT A SINGLE TRACK FOR SEVERAL SECONDS TO VERIFY THE MEDIA THIS IS NORMAL

4. AT THE END OF SCAN THE INTERRUPTER ARM SHOULD RETURN TO PARK POSITION (FIGURE 1) AND STAY THERE THEN THE READY LAMP SHOULD COME ON STEADILY



1.1 When the Pro-File first came out the firmware program used for the Z8 microprocessor on the Controller PCB was contained on a ROM chip located piggyback on the Z8. After this version had been out in the field awhile, it was found that due to the heat expansion that occurred when the machine was turned on, the leads from the ROM's piggyback socket were intermittently separating from the Z8.

Since the Z8 would be looking for program instructions when this happened, the temporarily open input would be interpreted as a bit in an instruction code and cause the Z8 to do strange things including putting the Pro-File into Write mode as the heads were doing a seek to a target track. This of course destroyed any sector header and/or data block fields that happened to be passing under the heads as they were on their way to the target track.

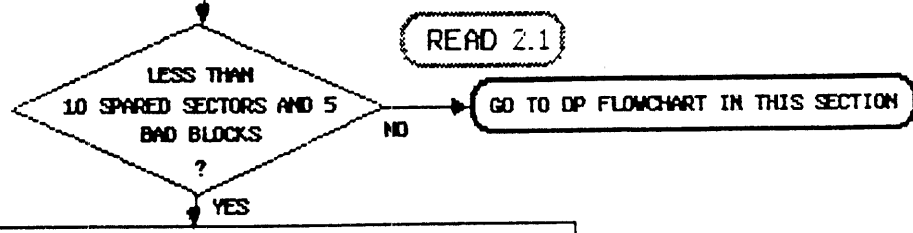
Later when a read of the damaged sectors was tried, either as a result of the next power up Scan operation, or a read command from the host computer system, the Z8 would detect the problem and ultimately spare the sector which of course made the malfunction look like a media problem.

The logical solution for the imagined media problem (the Z8 problem was not known at the time) was to replace the now badly formatted (though undamaged) HDA with a new HDA. This action would cause the Pro-File to work fine until the piggyback ROM again separated from the Z8. The HDA would be replaced again, ... etc.

Needless to say this process was not very effective. The **masked ROM Z8** has been developed to be an effective solution to this problem. All **piggyback Z8s** are to be replaced with this version. It is projected that most of the current Pro-File problems will be remedied by this upgrade. (Now return to the point in the flowchart which referred you to this discussion.)

1.2 All functions performed by the Controller and Analog PCBs and the HDA are ultimately controlled by the firmware program in the Z8 microprocessor on the Controller PCB. During power up on the Pro-File the Z8 will have the Pro-File go through a Scan operation in which certain specific things are checked for. A detailed explanation of the Scan operation may be found in Section 3 of this manual. (Now proceed to the **NoScan flowchart.**)

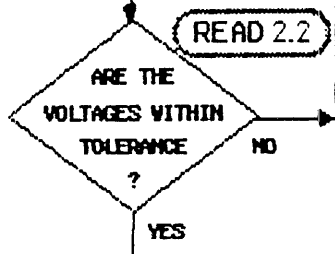
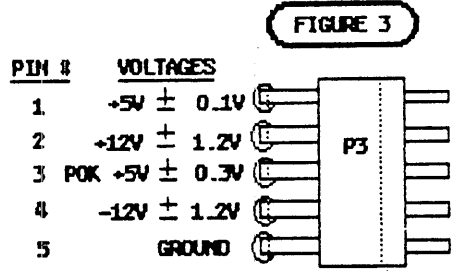
SHEET 2



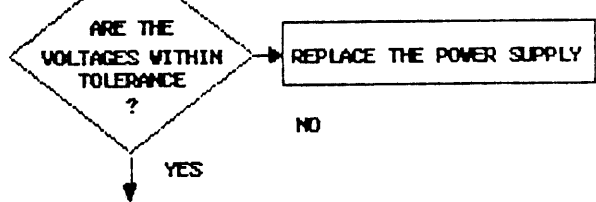
TURN OFF THE PROFILE THEN:

1. EXAMINE THE PCB'S FROM THE PROBLEM PROFILE FOR BENT PINS, BROKEN LEADS, CRACKED BOARDS, ETC.
2. INSTALL UPGRADES ON THE CONTROLLER AND ANALOG PCB'S, IF NECESSARY
3. CHECK & ADJUST THE HDA BRAKE AND INDEX SENSOR, IF NECESSARY (IF INSTRUCTIONS ARE NEEDED REFER TO SERVICE PROCEDURES)

TURN THE PROFILE ON AND MEASURE THE POWER SUPPLY VOLTAGES AT P3 OF THE CONTROLLER PCB (REFER TO FIGURE 3)



WHILE LEAVING EACH MODULE IN PLACE, DISCONNECT CONNECTORS J4, J3, AND J2 (J4 CONNECTS THE HDA TO THE POWER SUPPLY, J3 CONNECTS THE CONTROLLER PCB TO THE POWER SUPPLY, AND J2 CONNECTS THE CONTROLLER PCB TO THE ANALOG PCB) THEN CONNECT A KNOWN GOOD CONTROLLER PCB INTO J3 AND RECHECK EACH VOLTAGE



ONE AT A TIME, RECONNECT THE FOLLOWING:

IF THE PROBLEM REDOCCURS AFTER THE RE-ATTACHMENT OF A MODULE THEN THAT IS PROBABLY THE PROBLEM MODULE

1. J3 TO THE OLD CONTROLLER PCB
2. J2 TO THE OLD CONTROLLER PCB (POWER TO ANALOG PCB)
3. J4 TO THE HDA

GO TO SHEET 3

**2.1** The Quick Debugger program reads the Spares table on the Profile and prints the original sector location of every spared sector listed in that table. Additional information on sparing sectors may be found in the Special Function Tracks explanation in the HDA format description in the Appendices Section of this manual. At this point in the flowchart you know that Scan worked OK, but that the HDA has spared too many sectors. Spared sectors can be caused by either:

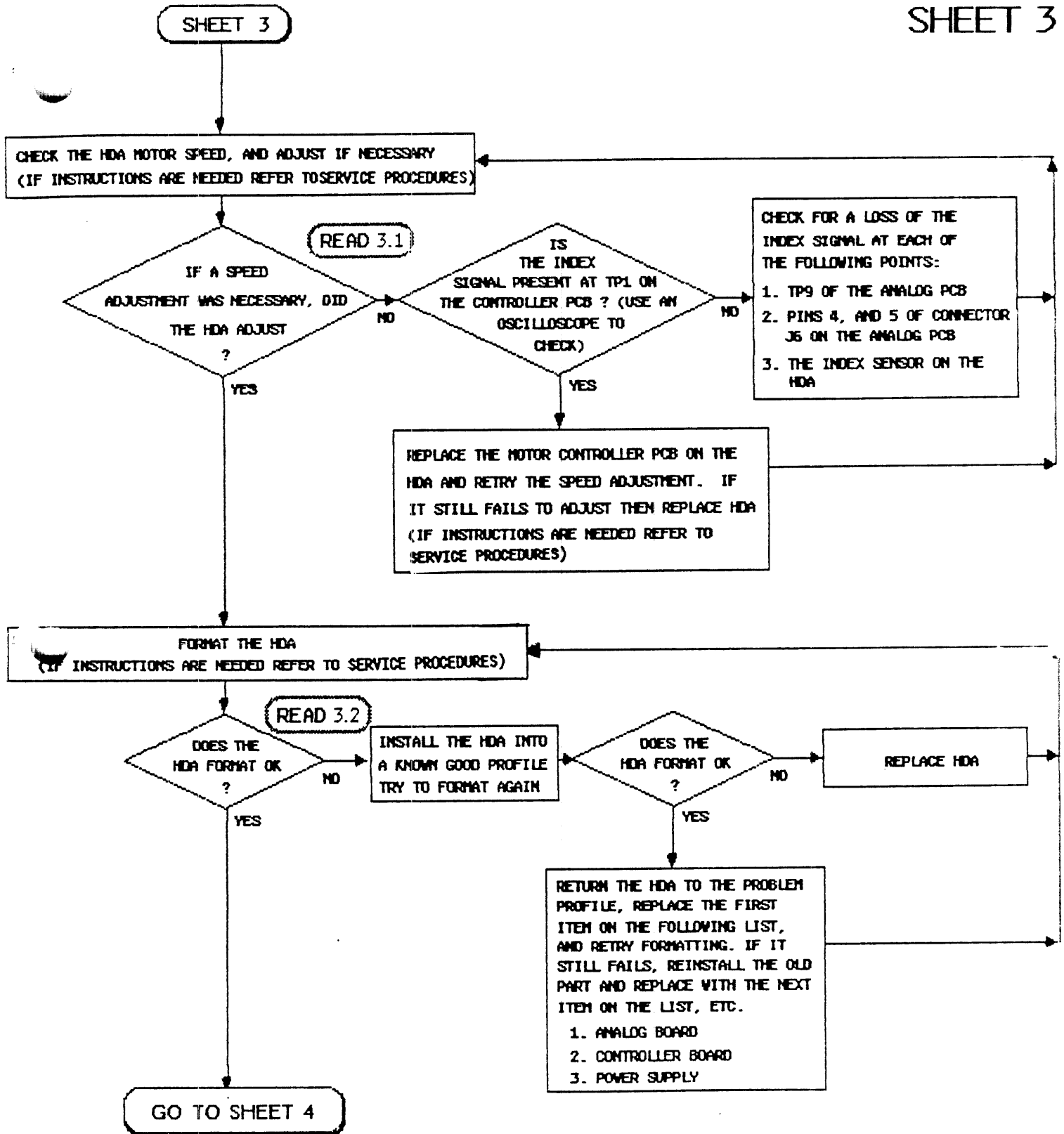
1. **Electronic problems** causing a sector to be unreadable or somehow alter its data bit pattern at the original sector location on the disk. For example the Z8 may have malfunctioned as it was performing a Seek, and instructed the electronics to write as the heads were moving across the media to a target track. This of course would destroy the parts of all the sectors that the head passed over on its way to the target track.
2. **Media problems** making it impossible to record magnetic information on a sector where it occurs. This could be a manufacturing defect in the media (the magnetic coating on the disk), or a ding in the media caused by head contact.

One way to determine whether a spared sector was caused by a media problem or an electronic problem is to continuously read the questionable sector and examine its analog signal with an oscilloscope. The Quick Debugger printout gives you a list of spared sectors that you might want to look at. The DP (Diagnostic Procedure) flowchart that you are being referred to, will explain how you can continuously read a spared sector and interpret its analog signal. (**Now proceed to the DP Flowchart.**)

**2.2** A missing or out of tolerance voltage can be caused by any of the modules in the Pro-File. The method used in this flowchart to isolate the problem module is to disconnect the power supply from all the modules, plug in a known good Controller PCB and monitor the voltages at P3 (the power supply connection to the Controller PCB). If the power supply is at fault then the voltage/s will still be missing or out of tolerance.

**WARNING:** At least one module must be connected to the Power Supply at all times to provide it with a load.

If the voltages are OK with the known good Controller PCB installed, then the problem must be with a module other than the power supply. To determine which of these modules is causing the power problem, each module is reconnected one at a time and P3 is checked after each reconnection. (**Now return to the flowchart.**)



**3.1** The Index signal is never actually used by the Pro-File electronics after the HDA has been formatted. During the format process, Index is used to provide a reference for the sectoring scheme to be put on the disk. (For an explanation of the Format used on the Pro-File refer to the Pro-File HDA Description in the Appendices section of this manual.)

But the Index does provide the technician with an indication of actual disk speed. It should occur once per revolution just before sector 0 on disk surface 0. Since the disk speed is supposed to be 3600 RPM this means that the frequency counter should measure a 16.666 ms period between each Index pulse.

If the Index signal is present at TP1 of the Controller PCB, but will not adjust as per directions in the Index Check and Adjustment procedure in the Service Procedures Section of this manual, then the problem could be with the electronics on the Motor Controller PCB on the HDA, or with the disk motor on the HDA. If the signal is absent at TP1 on the Controller PCB, then flow should be traced back to the Index sensor on the bottom of the HDA. (Now return to the point in the flowchart which referred you to this discussion.)

**3.2** During the Format process all sector headers and marks are erased and the spares tracks (track 77 on all disk surfaces) are erased. An inability to format could be caused by an electronic problem in the Pro-File, or by the HDA. If the HDA formats OK after putting it into a known good Pro-File, then the problem is probably with one of the electronics modules in the Pro-File. (Now return to the point in the flowchart which referred you to this discussion.)

SHEET 4

INSTALL THE SYSTEM Z8 AND RUN THE FINAL SYSTEM TEST (FST) ON THE PROFILE FOR 15 MINUTES  
(IF INSTRUCTIONS ARE NEEDED REFER TO SERVICE PROCEDURES)

15 MINUTE FST  
RUN WITHOUT FAILING  
SERVICE CRITERIA \*  
(PAGE 2.37)  
?

READ 4.1

DID THE  
FST ERRORS OCCUR  
ON THE SAME SECTORS AS  
THOSE FOUND DURING  
QUICK DEBUGGER  
TEST ?

NO  
RECORD THE NEW SECTORS THAT ARE  
DIFFERENT ON A LIST OF BAD SECTORS

GO TO THE DP FLOWCHART  
IN THIS SECTION

YES

YES

INSTALL THE COVER ON THE PROFILE, CONTINUE TO RUN  
FOR 48 HOURS.  
(IF INSTRUCTIONS ARE NEEDED REFER TO SERVICE PROCEDURES)

48 HOUR  
FST RUN WITHOUT  
FAILING SERVICE CRITERIA \*  
(PAGE 2.37)  
?

READ 4.1

DID THE  
FST ERRORS OCCUR  
ON THE SAME SECTORS OF  
THOSE FOUND DURING  
QUICK DEBUGGER  
TEST ?

NO  
RECORD THE NEW SECTORS THAT ARE  
DIFFERENT ON A LIST OF BAD SECTORS

GO TO THE DP FLOWCHART  
IN THIS SECTION

YES

YES

GOOD PROFILE

**4.1** The FST (Final System Test) is an exerciser/tester program used to determine whether or not the Pro-File is operating within acceptable limits.

For approximately the first 10 minutes of the FST, the data block field of every sector is written to and read to detect any CRC read errors.

The system Z8 is used during this test, so the same firmware routines (i.e. Scan, Seek, Read, Retry, Diagnostic, etc.) will be used. After the initial 10 minute write/verify has been performed, the FST exercises the Profile by doing random Seeks, Reads, etc. until its operation is terminated when the operator presses the <ESCAPE> key.

The reason the flowchart has you check for problems after the first 15 minutes of FST is because most hard failures will probably produce errors within 5 minutes after the FST begins to exercise the Pro-File. At this point in the flowchart errors can be caused by 2 types of problems:

1. An **Electronic problem** which has caused a sector to be unreadable by altering the data bit pattern at its original sector location on the disk. For example the Z8 may malfunction as it performs a Seek, and instruct the electronics to write as the heads move across the media to a target track.

This of course would destroy the parts of all the sectors that the head passes over on its way to the target track (the head should never write during a seek).

2. A **Media problem** which has made it impossible to record magnetic information on the sector where it occurs. This could be a manufacturing defect in the media (the magnetic coating on the disk), or a ding in the media caused by head contact during rough handling.

The big question at this point is which of the 2 types of problems described above is the real culprit. If the error was caused by an intermittent electronic problem producing a bad format on the HDA, then this looks like an HDA (media) problem. However, if the HDA is replaced the problem will probably reoccur in time. (This discussion is continued on the next page.)



**4.1** (continued) The method this flowchart uses to determine which type of problem caused the error is to compare the sector locations of sectors that had errors before formatting (a list of these sectors was printed out when you ran the Quick Debugger program on the problem Pro-File), with those produced after formatting (these will be shown by the FST).

If they are the same, then the problem which caused the errors, is probably bad media because bad media locations don't change, so the HDA should be replaced.

If they are different, then the problem is probably electronic. This is because it is highly unlikely that an intermittent electronics problem would occur on the same sector twice.

(If you would like further information on spared sectors, firmware routines, the Pro-File's HDA format, etc., you may refer to the descriptions in the Appendices Section of this manual.)

If the faulty sectors were the same, and the number of errors exceeds those specified by the FST service criteria sheet (found in the Service Procedures Section), then replace the HDA and return to the point in the flowchart which referred you to this discussion.

If they are different, then the problem is probably electronic and you need to look at some of the different faulty sectors to determine what is bad about them and so determine which module is faulty. The DP (Diagnostic Procedure) flowchart that you are being referred to, will explain how you can continuously read a spared sector and interpret its analog signal. (If there were different sectors, then proceed to the DP Flowchart.)

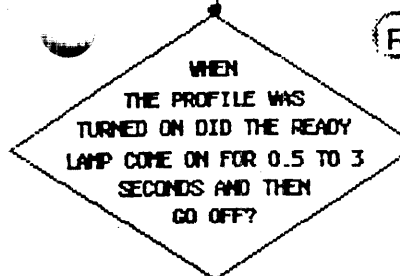
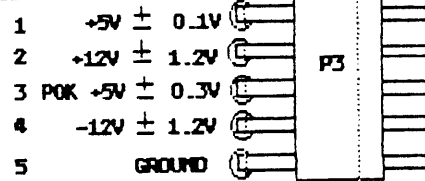
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# NO SCAN FLOWCHART

SHEET 1

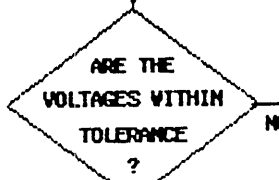
FIGURE 3

PIN # VOLTAGES

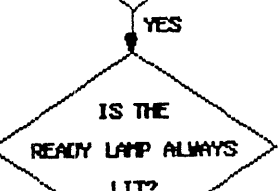


READ NS1.1

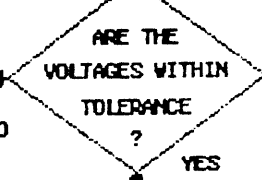
MEASURE THE POWER SUPPLY VOLTAGES AT P3 OF THE CONTROLLER PCB (REFER TO FIGURE 3)



WHILE LEAVING EACH MODULE IN PLACE, DISCONNECT CONNECTORS J4, J3, AND J2 (J4 CONNECTS THE HDA TO THE POWER SUPPLY, J3 CONNECTS THE CONTROLLER PCB TO THE POWER SUPPLY, AND J2 CONNECTS THE CONTROLLER PCB TO THE ANALOG PCB) THEN CONNECT A KNOWN GOOD CONTROLLER PCB INTO J3 AND RECHECK EACH VOLTAGE



REPLACE THE POWER SUPPLY



REPLACE THE FIRST ITEM ON THE FOLLOWING LIST. IF IT STILL FAILS, REINSTALL THE OLD PART AND REPLACE WITH THE NEXT ITEM

1. SYSTEM Z8
2. CONTROLLER PCB

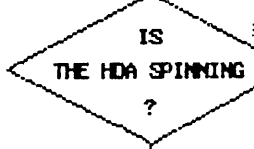
REPLACE THE FIRST ITEM ON THE FOLLOWING LIST. IF IT STILL FAILS, REINSTALL THE OLD PART AND REPLACE WITH THE NEXT ITEM

1. THE READY LED
2. CONTROLLER PCB

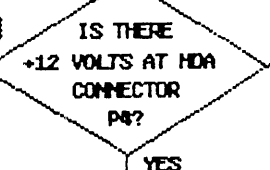
ONE AT A TIME, RECONNECT THE FOLLOWING:

IF THE PROBLEM REOCCURS AFTER THE RE-ATTACHMENT OF A MODULE THEN THAT IS THE SUSPECTED MODULE

1. J3 TO THE OLD CONTROLLER PCB
2. J2 TO THE OLD CONTROLLER PCB (POWER TO ANALOG PCB)
3. J4 TO THE HDA



READ NS1.2



REPLACE THE POWER SUPPLY

TURN OFF THE PROFILE REPLACE THE MOTOR CONTROLLER PCB, IF THAT DOESN'T WORK, THEN REPLACE THE HDA

GO TO SHEET 1 OF THE MAIN FLOWCHART PG 1.4

GO TO NO SCAN FLOWCHART SHEET 2

**NS1.1** Upon power up on the Pro-File the Z8 will wait for the POK (Power OK) signal to occur. This signal is generated by the power supply when it determines that the proper voltage levels for each voltage have been reached and stabilized. When it happens the Z8 will cause the Ready lamp to extinguish. This should happen within 1/2 to 3 seconds of power up.

A missing or out of tolerance voltage can be caused by any of the modules in the Pro-File. The method used in this flowchart to isolate the problem module is to disconnect the power supply from all the modules, plug in a known good Controller PCB and monitor the voltages at P3 (the power supply connection to the Controller PCB). If the power supply is at fault then the voltage/s will still be missing or out of tolerance.

If the voltages are OK with the known good Controller PCB installed, then the problem must be with a module other than the power supply. To determine which of these modules is causing the power problem each module is reconnected one at a time and P3 is checked after each reconnection. (Now return to the point in the flowchart which referred you to this discussion.)

**NS1.2** Approximately 20 seconds after the Ready lamp goes out indicating that the power has stabilized, the disk motor should be rotating at 3600 RPM (its operating speed). If the HDA isn't spinning the Pro-File can't read data and that's probably why the Scan operation was unsuccessful. (Now return to the point in the flowchart which referred you to this discussion.)

NO SCAN FLOWCHART  
PAGE 2

READ NS2.1

AFTER THE HDA COMES UP TO SPEED (ABOUT 20 SEC) DOES THE INTERRUPTER ARM MOVE TO TRACK 0 AND BEGIN STEPPING ?

REPLACE THE FIRST ITEM ON THE FOLLOWING LIST: IF IT STILL FAILS, REINSTALL THE OLD PART AND REPLACE THE NEXT ITEM ON THE LIST.

1. CONTROLLER PCB WITH GOOD SYSTEM Z8
2. ANALOG PCB
3. POWER SUPPLY
4. EXAMINE HDA FOR PROBLEMS, REPLACE IF NECESSARY

GO TO SHEET 1 OF MAIN FLOWCHART

YES

READ NS2.2

DOES THE INTERRUPTER ARM STEP FROM TRACK TO TRACK BUT PAUSE FOR MORE THAN ONE MINUTE AT ANY TRACK POSITION?

THE SCAN MUST HAVE TAKEN LONGER THAN 90 SECONDS.

1. INSTALL THE DEBUGGER Z8
2. LOAD THE DEBUGGER PROGRAM INTO AN APPLE /// TYPE <RTOSOH> THEN PRESS <RETURN>
3. TYPE <R>, <Space>, <+S>, <Space>, <PE>, <Space>, <X>, THEN PRESS <RETURN>

NOTE:

ALL 0's ARE ZERO's

OBSERVE:

- a. THAT THE INTERRUPTER ARM STEPS THROUGH EACH TRACK FROM 0 TO PARK
- b. IF AN ERROR OCCURS THE PROGRAM STOPS WITH THE SECTOR SHOWN ON THE CRT

4. IF AN ERROR OCCURS AND THE PROGRAM STOPS RECORD THE SECTOR ON A BAD SECTOR LIST FOR USE IN THE DIAGNOSTIC PROCEDURE

5. CONTINUE THE PROCEDURE DESCRIBED ABOVE UNTIL YOU HAVE RECORDED 10 BAD SECTORS OR UNTIL THE INTERRUPTER ARM HAS GONE FROM TRACK 0, TO PARK POSITION, TO TRACK 0 AGAIN

YES

GO TO DP FLOWCHART IN THIS SECTION

**NS2.1** The firmware program in the system Z8 waits approximately 20 seconds after a successful powerup (a successful powerup is indicated by the Power OK signal becoming active and causing the Ready lamp to extinguish) before it initiates the Scan operation. During Scan operation the Z8 will cause the following things to occur.

Note: Turn off the Pro-File and gently position the interruptor arm to the Park position (if it is not already there). Then turn on the Pro-File while you observe the following.

The interruptor arm will move to approximately the center of its travel and pause there briefly while the spares table is read from track 77 on disk surfaces 2 or 3.

If there is a problem which disables the Pro-File from being able to read anything, then this is the first place that it would be evident.

If the Z8 is unable to read sector headers on track 77, then the interruptor arm may go to track 0 and back to 77 to try again. If it still can't read sector headers it may go to track 155 (Park position) and back to track 77 to try again to attempt read the spares table. If it still can't read the spares table the Z8 will abandon the Scan operation and move the interruptor arm to Park position.

(If you would like a detailed description of the Scan operation, or further information on the spares table, error recovery routines, the Pro-File's HDA format, etc. refer to the descriptions in the Appendices Section of this manual.)

(Now return to the point in the flowchart which referred you to this discussion.)

**NS2.2** If the Seek to track 77 was successful (as described above in NS2.1), then the read circuitry must be at least marginally OK, so the Z8 will go to track 0 to begin to read each sector in sequence beginning with sector 0. During this time the Ready lamp will blink. If there is a problem in this procedure the Pro-File firmware may go to an error recovery routine.

(If you would like a detailed description of the Scan operation, or further information on the spares table, error recovery routines, the Pro-File's HDA format, etc. refer to the descriptions in the Appendices Section of this manual.)

(Now return to the point in the flowchart which referred you to this discussion.)

# DP - DIAGNOSTIC PROCEDURE

**NOTE:** The Diagnostic Procedure (DP) flowchart begins on page 1.22. However if this is your first time through this procedure, it is strongly recommended that you read the following introduction.

## Introduction:

The main objective of this procedure is to familiarize the technician with some common failure modes within the Pro-File electronics. Each of these modes usually shows up as an alteration, of the analog waveform of the sector being read from the HDA.

The modified patterns usually do not reflect actual physical damage to the disc surface, but rather a problem in the Pro-File electronics.

The technician's job will be to examine the faulty sector's analog signal as it is being read to determine which module within the Pro-File caused or is causing the failure.

The faulty sector's analog signal waveform can be monitored directly by placing oscilloscope probe(s) on either Test Points 1 & 2 (TP1 & TP2 are the same signal differentiated) on the Analog PCB and externally triggering the scope with the Index signal at TP9.

An easy way to access these test points is to remove the metal plate located underneath the Pro-File, and tilt the Pro-File up on its side to expose the Analog PCB (refer to page 2.22 for the location of the Test Points). This way the Pro-File can be checked quickly with a minimum of disassembly.

Following this introduction are examples of analog signals PCB taken on TP1 & TP2 along with the VCO charge pump data locking error voltage at TP8.

The signal read at either TP1 or TP2 is the analog data read directly from the head after passing the data through a preamplifier, lo-pass filter, and automatic gain control circuit.

The signals at TP1 and TP2 are really just head signals amplified by the circuitry on the Analog PCB. A loss of signal at these test points may indicate that there is a problem with the connection between the HDA and Analog PCB, or the Analog PCB circuitry.

(continued on the next page)

## Introduction: (continued)

The signal obtained from TP8 is the feedback voltage that a Phase Locked Loop (PLL) control circuit uses to lock to the analog data signal on the HDA.

The feedback either increases or decreases the voltage to a **Voltage Controlled Oscillator (VCO)** causing it to increment or decrement its output frequency thereby syncing that frequency to that of the data being read.

When the Pro-File is idle, the VCO locks to about 20 Mhz, or twice the Controller PCB clock frequency (there is very little signal at TP8).

When reading, the frequency varies in proportion to the data frequency written to the disc.

So, whenever the Pro-File is reading the data from the HDA, the signal will change in amplitude to reflect data on the disc. (refer to page 1.26, Example of Normal VCO charge pump Signal {TP8 voltage})

### Possible Problems:

#### **A. Z8 microprocessor**

Of the problems existing in the Pro-File, most of them can be attributed to the system Z8 microprocessor on the Controller PCB. (Refer to page 1.5, part 1.1).

The older system Z8 was a "piggyback" type chip, and the new version is the masked system Z8.

The masked version is a much improved version less likely to fail over a normal Pro-File lifetime, yet, there is small percentage of fallout within these chips too.

One malfunction that commonly occurs is when the Z8 turns on the write circuitry while seeking to a different track. (Refer to the following pages on Damaged or Cleared Data Areas)

(continued on the next page)



## Introduction: (continued)

### Possible Problems: (continued)

#### B. Controller and Analog PCB Upgrades

In the past some lines on the Controller and Analog PCBs were being spuriously activated. Sometimes this would cause the Z8 to go into its write routine when it was supposed to be seeking or idle.

The Controller and Analog PCB upgrade procedures (described in the Service Procedures Section), were designed to be a solution to these problems.

#### C. Controller PCB

The Pro-File Controller PCB functionally provides control signals to the Analog PCB and HDA to move the heads to the proper track, select the proper sector, channel data, and monitor error conditions during a read or write.

If a malfunction occurs in any of these functions, the Controller PCB can be suspected as the bad module. However, do not forget to verify the Z8 microprocessor first.

#### D. Analog PCB

There are 2 main Analog PCB problems:

1. PLL (Phase Lock Loop) problems may show up as an abnormal VCO (Voltage Controlled Oscillator) charge pump signal at TP8 when the analog data signal at TP2 and TP2 appears normal. In this case, the PLL circuitry would not be able to lock to the analog data signal coming from the HDA. (Refer to page 1.40, Example of Abnormal VCO charge pump).
2. AGC (Automatic Gain Control) circuitry problems may <sup>cause</sup> the analog data signal to be low or non-existent at TP1 and TP2. (Refer to page 1.42, Example of Abnormal AGC signal)

#### E. Hard Disk Assembly (HDA)

Of the many possible problems which can occur on the HDA, there are four major ones.

(continued on the next page)

## Introduction: (continued)

### Possible Problems:

#### E. Hard Disk Assembly (HDA) (continued)

1. **Media damage** (Refer to page 1.38, Example of Bad Media) can be found by finding an area on the media with a loss of signal (not a sector mark), where repeated attempts at rewriting data does not return the area to normal. (Rewriting the sector can be accomplished with the Big Debugger program, using the <W> command, refer to page 2.40 for instructions)

There also can be damage to the media where one of the disc heads has struck the surface of the disc. Remember that there is a space for 32 bad sectors in the Spares Table, so a few bad sectors existing due to a media problem is acceptable and a normal part of Pro-File operation.

2. **Motor Speed problems** usually occur because of a defective Motor Control PCB on the HDA. A widely oscillating speed might adversely affect the operation of the Pro-File. The analog signals will be present at the Test Points, but the analog to digital circuitry will probably not be able to lock to the data on the HDA. And the Pro-File probably will not pass reformatting without errors occurring.
3. **Disc Head problems** are usually limited to a complete loss of signal at one or more of the heads. It is because of damage to the heads or a bad connection to the heads. Either way, the HDA needs replacement, as there is no way to repair a problem internal to the HDA in the field.
4. **Stepper Motor problems** may be caused by a bad connection between the Controller or Analog PCB's, or a bad stepper motor winding. Either way, the stepper will not move smoothly or have accuracy at any track step. To confirm the problem use the Read command from the Big Debugger program in the Service Procedures Section to perform a read on some track other than where the heads are now. If the interrupter arm rotates in the direction opposite of the target track, or shakes back and forth there may be a problem with the stepper motor.

Another problem that can occur is stepper motor **hysteresis**. Hysteresis is where a magnetic field is built up inside the stepper motor coils causing the motor to settle with the head positioned at a slightly off track position. In this case the HDA should be replaced since this is a track alignment problem internal to the HDA and not repairable by the technician.

DIAGNOSTIC PROCEDURE  
FLOWCHART

1. INSTALL THE DEBUGGER Z8 ON THE CONTROLLER PCB
2. CONNECT THE PROFILE TO AN APPLE /// (INTERFACE CARD IN SLOT 1)
3. BOOT THE BIG DEBUGGER PROGRAM

DO YOU  
HAVE A LIST OF FAULTY  
SECTORS  
?

YES

NO

READ DP 12

TYPE: <RT>H<y>S<z> WHERE x=THE TRACK, y=HEAD,  
z=SECTOR OF ONE OF THE SPARED OR BAD BLOCKS  
ON THE LIST, THEN PRESS <RETURN>

TYPE: <R> <SPACE> <X>, THEN PRESS <RETURN>

THE HDA SHOULD ATTEMPT TO STEP TO THE TRACK AND  
AND SECTOR JUST SPECIFIED AND CONTINUOUSLY READ.

READ DP 1.1

TYPE: <RTOHOS0>, FOLLOWED BY <RETURN>

TYPE: <R> <SPACE> <+S> <SPACE> <PE> <SPACE> <X>

THE HDA SHOULD STEP TO TRACK ZERO AND STEP  
TOWARDS PARK POSITION, INCREMENTING BY SECTORS.

IF THERE IS AN ERROR IN READING, THE BIG DEBUGGER  
PROGRAM WILL STOP THE PROFILE.

RECORD THE LOCATION OF THE SECTOR WHICH CAUSED THE  
ERROR, THEN PRESS <ESCAPE>

PERFORM THE STEPS IN DP 1.2 WHERE x=TRACK, y=HEAD,  
AND z=SECTOR FOR THE SECTOR WHICH CAUSED THE  
BIG DEBUGGER TO PAUSE ON ERROR

Note:

The 0's below  
are ZEROS.

CONTINUE WITH *OSCILLOSCOPE SETUP* OF  
DIAGNOSTIC PROCEDURE

**DPl.1** If you do not have a list of faulty sectors, then the interrupter arm must have spent 1 minute or more over a track during Scan. This probably means that the Pro-File had difficulty reading a sector or sectors on that track. By entering the commands specified at this step in the flowchart into the Big Debugger program; you will cause the Big Debugger program to read every sector in sequence and stop in the event of an error.

When the program stops the test operation, the heads will be positioned over the problem track, and the head for the disk surface containing the problem track will be enabled. This means that the analog signal from that track should continuously be sent to TP1 and 2 on the Analog PCB. Perform the steps in the DPl.3 procedure to view the signal from this track and determine if its display can provide you with a clue as to what the problem is.

If you don't feel that the display of this track is providing you with the symptoms you need to diagnose the problem, you can press the <SPACE> bar to cause the Big Debugger program to test the rest of the sectors until it finds another error. View that tracks signal for symptoms in the same way ....  
etc.

**DPl.2** By entering the commands specified at this branch in the flowchart into the Big Debugger program you will cause the Big Debugger program to read one of the sectors that you determined earlier in the flowchart might contain clues to electronic problems in the Pro-File.

While the program continuously reads the specified sector, the heads will be positioned over the problem sector's track, and the head for the disk surface containing the problem sector will be enabled. In DPl.3 you will find a procedure to view the signal from this track.

If you position your timebase delay highlight over the analog data read signal for this period and enter timebase delay mode on your oscilloscope you will see an expanded display of the questionable sector. Compare the display of the faulty sector by itself with the faulty sector examples later in this procedure to help you find the problem.

If you don't feel that the display of this sector is providing you with any of the symptoms described in DPl.3, you can enter the commands necessary to have the Big Debugger program continuously read the next faulty sector on your list. View that sectors signal for symptoms in the same way .... etc.

DIAGNOSTIC PROCEDURE  
OSCILLOSCOPE SETUP

READ DP 1.3

TO VIEW THE TRACK BEING READ:

1. TURN ON THE OSCILLOSCOPE AND ALLOW IT TO WARM UP FOR 15 MINUTES
2. *INITIALLY* SET CHANNEL A (OR 1) ON THE OSCILLOSCOPE TO THE FOLLOWING:
  - A. VOLTS PER DIVISION CONTROL SETTING TO 1 VOLTS/DIV
  - B. AC COUPLING
  - C. CONNECT TO HDA ANALOG DATA - TP1 OR 2 ON ANALOG PCB (GROUND THE PROBE)
3. SET CHANNEL B (OR 2) TO:
  - A. 0.5 VOLTS/DIV
  - B. AC COUPLING
  - C. CONNECT TO HDA VCO SIGNAL - TP8 ON ANALOG PCB (DO NOT GROUND THE PROBE)
4. USE EXTERNAL TRIGGER AND SET TIMEBASE TO:
  - A. 2  $\mu$ SEC/DIV
  - B. CONNECT EXTERNAL TRIGGER TO INDEX PULSE - TP1 ON CONTROLLER PCB
  - C. AUTO TRIGGERING - ADJUST TRIGGER LEVEL TO LOCK SIGNAL ON SCOPE

NOTE: IF THERE IS NO INDEX PULSE ON TP1 (CONTROLLER PCB), TRY USING TP9 (ON ANALOG PCB). IT IS ACTUALLY THE INDEX SIGNAL FROM THE HDA, IF IS NOT PRESENT, CHECK THE INDEX SENSOR ADJUSTMENT DESCRIBED IN SECTION 2

OBSERVE: THE SIGNAL YOU ARE VIEWING SHOULD BE SIMILAR TO THAT SHOWN IN THE PHOTOGRAPH ON THE OPPOSITE PAGE.

TO VIEW THE SECTOR BEING READ:

5. WHILE IN THE MAIN TIMEBASE, POSITION AND ADJUST THE DELAYED TIMEBASE HIGHLIGHT OVER THE PERIOD OF THE VCO CHARGE PUMP SIGNAL THAT IS ACTIVE (PROBABLY LOW AND OSCILLATING, SIMILAR TO THE LOWER SIGNAL IN THE PHOTOGRAPH ON THE OPPOSITE PAGE).
6. ENTER THE DELAYED TIME BASE TO VIEW THE QUESTIONABLE SECTOR

OBSERVE: THE SIGNAL YOU ARE VIEWING MAY BE COMPARED WITH THE NORMAL SIGNAL ILLUSTRATION SHOWN ON PAGE 1.28.

7. VIEW THE EXAMPLE SIGNALS IN THE FOLLOWING PAGES TO DETERMINE A PROBLEM WITHIN THE PROFILE

CONTINUE WITH DIAGNOSTIC PROCEDURE  
SIGNAL EXAMPLES

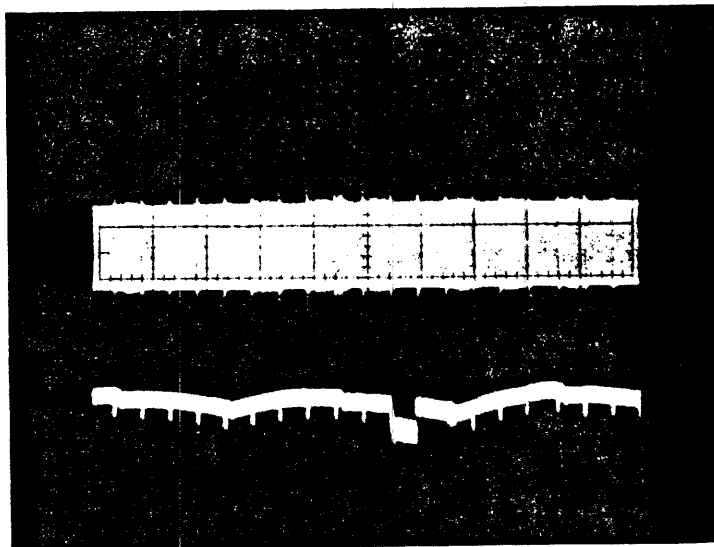
**DPl.3** At this point in the flowchart a head should be enabled over a track containing a faulty sector. On your oscilloscope display you should see a signal similar to that in the figure shown below.

If you had a list of faulty sectors, then the Big Debugger program should be continuously reading a faulty sector. Notice the period in the VCO charge pump signal where it is low and oscillating. The sector where the VCO charge pump signal goes low is the sector that is being read.

If you position your delay trigger highlight over the analog data read signal for this period and enter delay trigger mode on your oscilloscope you will see an expanded display of the questionable sector. Compare the display of the faulty sector by itself with the faulty sector examples later in this procedure. If you find one that is similar, read the corresponding explanation and if you wish perform the recommended module replacement.

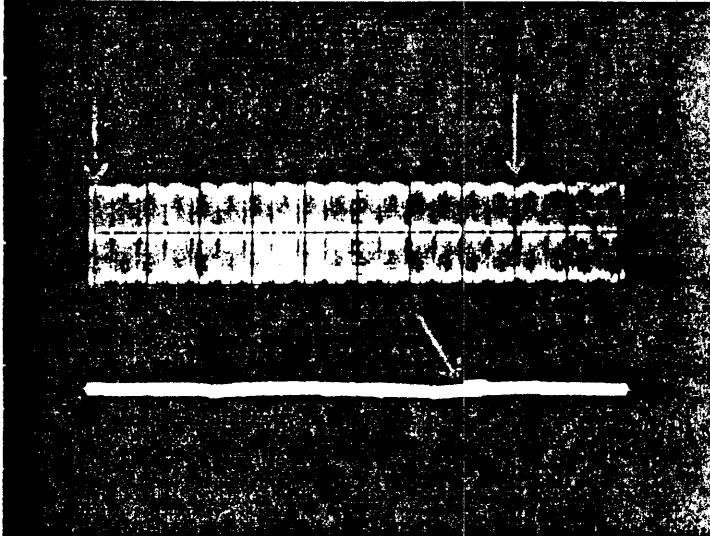
If you are viewing a questionable track and you don't know which sector is bad, then use the delay trigger function on your oscilloscope to view the sectors individually to determine why the Pro-File had a problem with this track.

**Note:** A sector mark (sometimes called sector gap) separates each sector as shown below. If you would like information on the format used for the Pro-File refer to the Pro-File HDA description in section 3.



# Diagnostic Procedure

## Example of a Normal Track



TP1 displays a view of a track of data. An entire track is shown between the arrows. Amplitude is 2 v peak to peak.

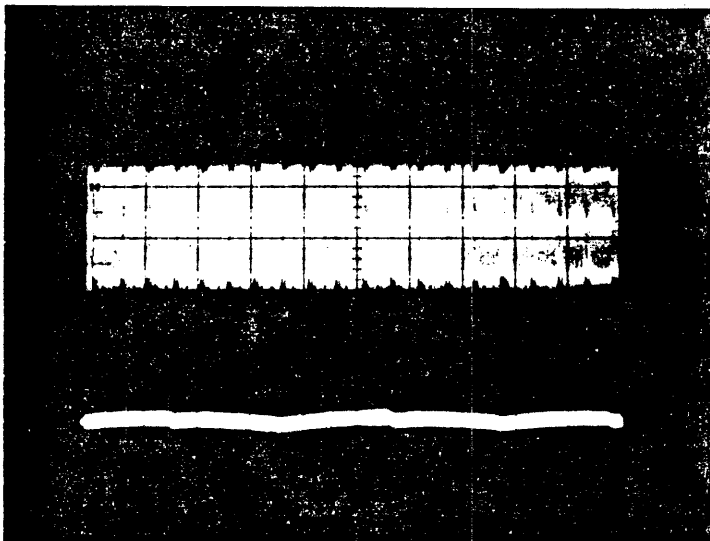
TP8 (VCO) is shown locking in to read a sector by the lower arrow.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div



TP1 displays another look at a normal track with a higher amplitude of 2.4 v. Note that there are 16 areas of no signal corresponding to the sector marks.

TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div

### Examples of a Normal Track

The amplitude voltage of an analog data signal from a normal track can vary depending on the physical location of the track, the Analog PCB, and what actual data has been written to the HDA.

The photos shown at the left are two characteristic normal tracks which show a **possible** variation in amplitude voltage. The upper photo displays an amplitude of about 2 volts peak to peak, the lower amplitude 2.4 volts.

Each track contains 16 sectors separated by a sector mark, but at this timebase the photo actually shows more than the 16 sectors.

This is because the period of signal displayed at this timebase is longer than the period of time that it takes to read one complete track, so the beginning of the same track is displayed as the disk begins its next rotation.

One complete track is shown between the arrows.

**Note:** Careful examination of the upper photo shows the VCO charge pump circuitry locking in on the sector indicated by the lower arrow.



## Examples of a Normal Sector

As explained in the previous example of a normal track, the amplitude voltage of an analog data signal from a normal track can vary depending on the physical location of the track, the Analog PCB, and what actual data has been written to the HDA.

The illustration at the left shows a typical view of a normal sector's analog signal. The amplitude of a sector can vary from about 1.1 volts to over 2 volts.

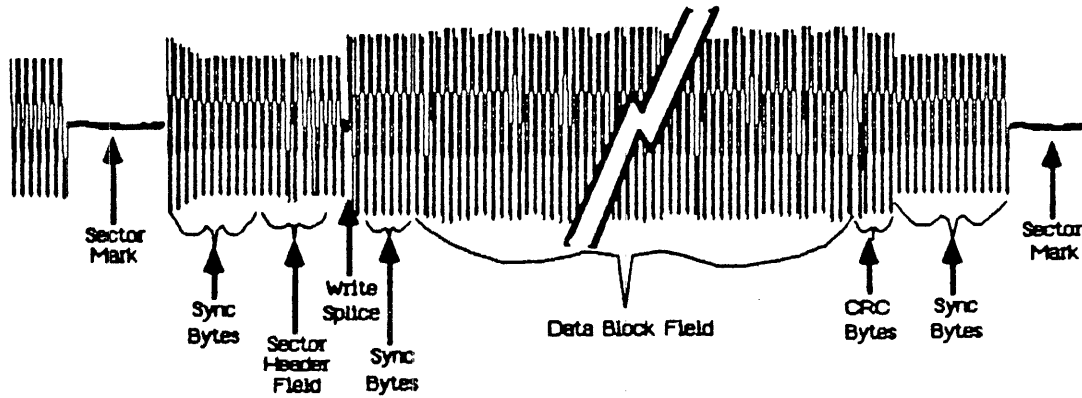
The flared "bell" shape at the beginning of each sector, is a normal characteristic caused by the AGC (Automatic Gain Control) circuitry as it adjusts for the gain of the analog read signal from the head. If the bell shape is missing, the technician might suspect a faulty Analog PCB.

The Sync bytes and Sector Header field at the beginning of the sector are written during formatting, and should never be written over after formatting. The Write Splice is the point at which the Pro-File will normally begin to write a data block into the sector.

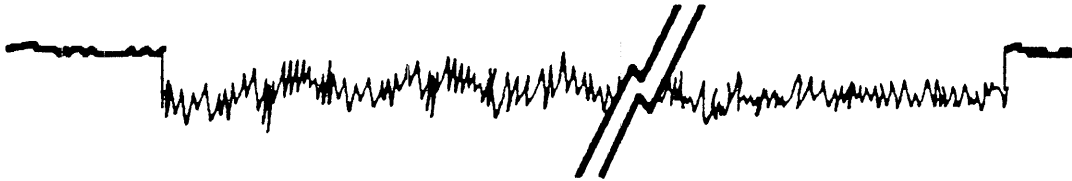
When the Pro-File reads a data block from a sector the data block field may not be in exact sync with the Sector Header field, so additional sync bytes are needed after the Write Splice, for the Pro-File to sync to the data field.

Notice that the VCO charge pump signal at TP8 goes low only for the sector being read. The oscillations that occur while the charge pump signal is low reflect the changes the VCO (Voltage Controlled Oscillator) makes to sync with the clock in the analog data signal read from the HDA (TP 1 or 2).

## EXPANDED VIEW OF ONE SECTOR (TP 1 or 2)



## EXPANDED VIEW OF VCO CHARGE PUMP SIGNAL (TP8)



THE OSCILLATIONS SHOULD OCCUR ONLY FOR THE SECTOR BEING READ.  
THE VOLTAGE LEVEL THEY OCCUR AT DEPENDS ON THE SPEED ADJUSTMENT  
ON THE HDA MOTOR CONTROL PCB (THE ILLUSTRATION DEPICTS A SIGNAL  
RIDING ON A NEGATIVE LEVEL, AS MOST WILL)

### Example of a Normal VCO charge pump Signal

As explained in this flowchart's introduction, the VCO charge pump signal at TP8 enables the VCO (Voltage Controlled Oscillator) on the Analog PCB to synchronize to the data written on the disk.

The voltage level at TP8 causes the VCO to increase or decrease its output frequency.

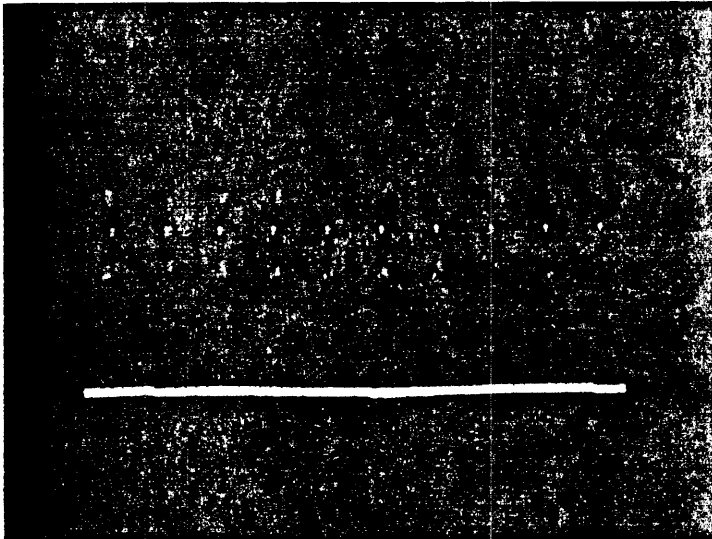
When the Z8 wishes to read a sector on a track this signal will go low and then oscillate. This means it is now controlling the correction of the VCO as needed during the reading of the sector.

After the sector is read, the Z8 will direct the signal to go high again since there is no longer any data to be synced to.

The upper photo shown at the left shows a view of about half of a normal track. The Pro-File was told (using the Big Debugger Program) to read the sector continuously. No read errors occurred despite the large amplitude signal seen on TP8.

The lower photo displays an enlarged view of the sector being read above. Note that the changes in peaks in the data signal at TP1 correspond to the peaks in the VCO charge pump signal in TP8. An even larger view of the signals would show this more clearly.

## Diagnostic Procedure



### Example of a Normal VCO Signal

TP1 displays a partial view of a track of data. The Profile has been told to read the sector of data shown by arrow.

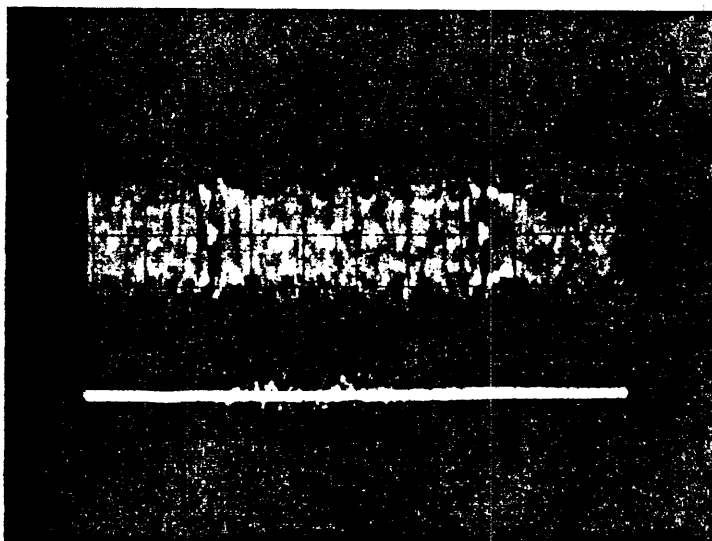
TP8 (VCO) shows a signal corresponding to the sector read. This signal "locks" to the data.

#### Scope Settings:

TP1 - 1 volt/div

TP8 - .2 volt/div

Timebase: 1 msec/div



TP1 displays a larger view of the sector being read.

TP8 (VCO) shows a more detailed look at the signal produced at TP8. Each increase and decrease in signal amplitude corresponds to the data signal at TP1.

#### Scope Settings:

TP1 - 1 volt/div

TP8 - .2 volt/div

Timebase: .2 msec/div

### Example of Damaged Track

As described in the Pro-File HDA Format description in section 3, sector marks divide each track into 16 separate sectors. The Controller PCB expects the sectors to be in a certain location with respect to the sector marks.

The upper photo shown at the left shows an entire track of data with uneven length sectors (they should all be the same length), and extra pulses (TP1). A normal sector would occur where the VCO charge pump (at TP8) shows the amplitude in the negative direction (down).

The Pro-File was instructed to read all the sectors of the track with the Big Debugger program, what is shown is every other sector being read. The lower photo shows an enlarged view of the track analog signal displaying areas which appear to be similar to a normal sector, but are actually damaged.

There are extra areas of no signal similar to a normal sector mark at the end of some of the sectors, and areas with multiple sector marks at the beginning of the sector (refer to lower arrow).

At this point, the technician would normally suspect the system Z8 as the cause of the damaged tracks. This is because the Z8 has historically been the most common failed component in the Pro-File. Yet, this Pro-File already had a masked version of the system Z8 installed on the Controller PCB.

So it is a possibility that the Controller PCB is really at fault, not the Z8. Since the Z8 had already been replaced during the upgrade procedures, it was decided to reformat the HDA (correcting the track damage in the format), and run FST for 15 minutes to see if the track damage would reoccur. A replacement system Z8 was installed, the system upgraded, and the HDA reformatted.

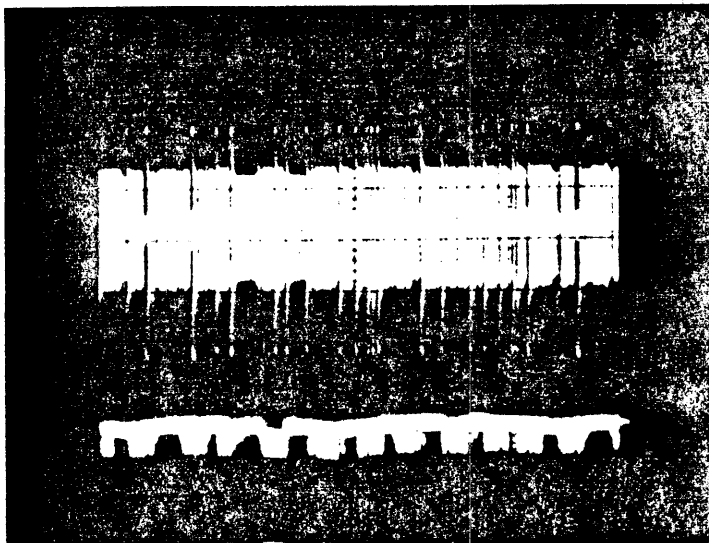
After running FST for 10 minutes, the Pro-File began to produce errors: (Refer to page 2.37 for a list of errors and criteria for failure)

```
04 00 00 00
05 00 00 00
15 80 00 00
```

The Pro-File was stopped and the Controller PCB replaced. (The original Z8 was reinstalled into the new Controller PCB) and the 15 minute FST rerun. No additional errors occurred even after 48 hours, so it was assumed that the Controller PCB somehow produced the damaged tracks.

# Diagnostic Procedure

## Example of a Damaged Track



TP1 displays a view of a track of data. There appears to be extra sectors if you count the extra peaks.

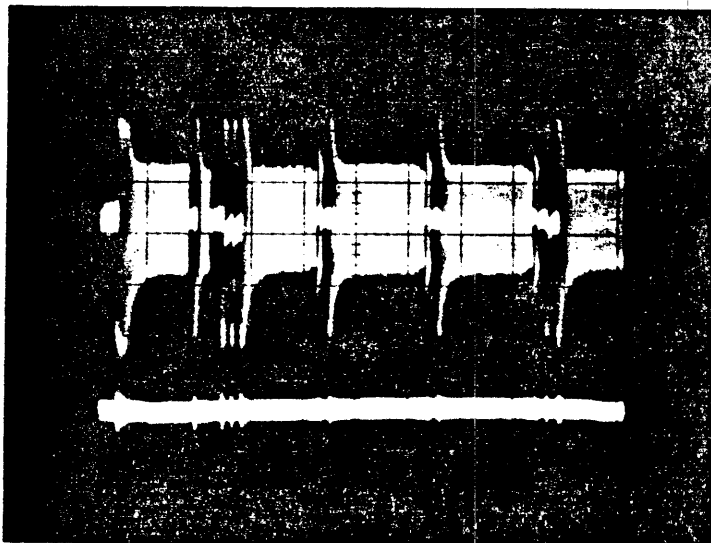
TP8 (VCO) attempted to lock to the data present on the track, but was unable to confirm any good sectors.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div



TP1 displays a closer view of some of the sectors of the track. Several sectors appear to be normal, but have actually been damaged.

TP8 (VCO) could not lock to the damaged the sectors.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

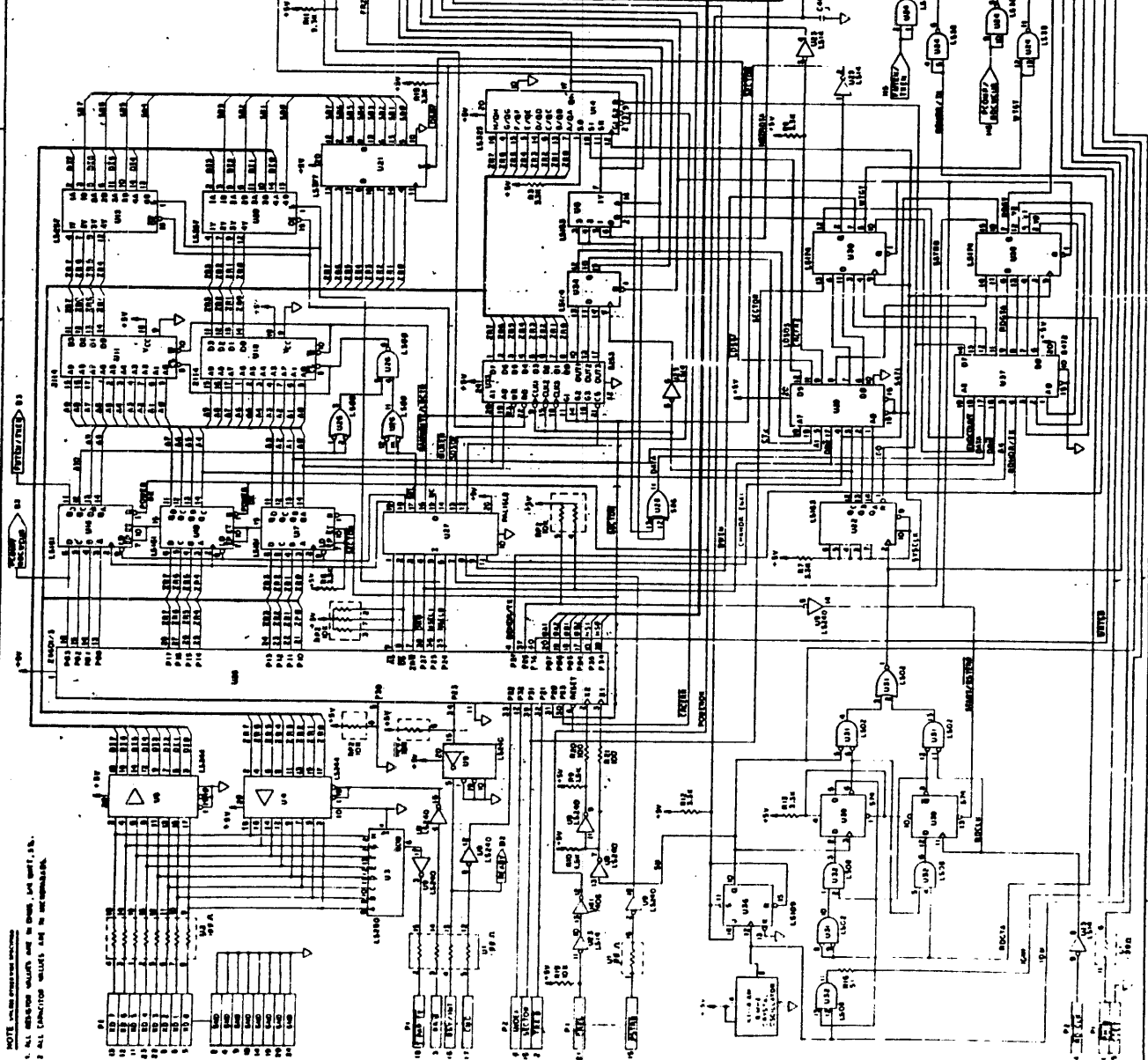
Timebase: .5 msec/div

### Suspect:

1. System Z8
2. Controller Board
3. HDA

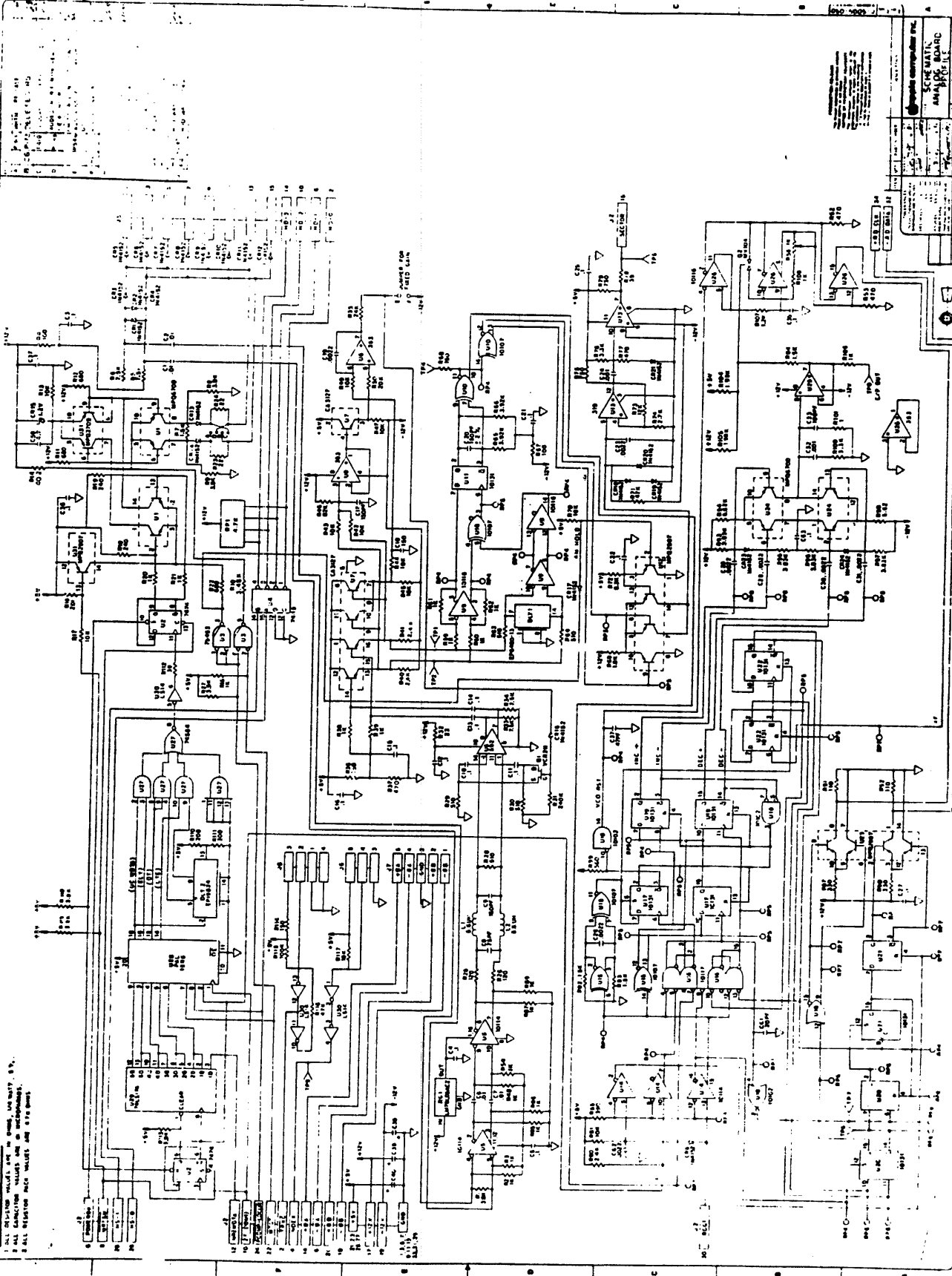
REV	DESCRIPTION	DATE	BY	CHKD
1	INITIAL DESIGN	10/15/68	J. W. B.	
2	REVISED TO ADD...	10/22/68	J. W. B.	
3	REVISED TO ADD...	11/05/68	J. W. B.	
4	REVISED TO ADD...	11/12/68	J. W. B.	
5	REVISED TO ADD...	11/19/68	J. W. B.	
6	REVISED TO ADD...	11/26/68	J. W. B.	
7	REVISED TO ADD...	12/03/68	J. W. B.	
8	REVISED TO ADD...	12/10/68	J. W. B.	
9	REVISED TO ADD...	12/17/68	J. W. B.	
10	REVISED TO ADD...	12/24/68	J. W. B.	
11	REVISED TO ADD...	1/01/69	J. W. B.	
12	REVISED TO ADD...	1/08/69	J. W. B.	
13	REVISED TO ADD...	1/15/69	J. W. B.	
14	REVISED TO ADD...	1/22/69	J. W. B.	
15	REVISED TO ADD...	1/29/69	J. W. B.	
16	REVISED TO ADD...	2/05/69	J. W. B.	
17	REVISED TO ADD...	2/12/69	J. W. B.	
18	REVISED TO ADD...	2/19/69	J. W. B.	
19	REVISED TO ADD...	2/26/69	J. W. B.	
20	REVISED TO ADD...	3/05/69	J. W. B.	
21	REVISED TO ADD...	3/12/69	J. W. B.	
22	REVISED TO ADD...	3/19/69	J. W. B.	
23	REVISED TO ADD...	3/26/69	J. W. B.	
24	REVISED TO ADD...	4/02/69	J. W. B.	
25	REVISED TO ADD...	4/09/69	J. W. B.	
26	REVISED TO ADD...	4/16/69	J. W. B.	
27	REVISED TO ADD...	4/23/69	J. W. B.	
28	REVISED TO ADD...	4/30/69	J. W. B.	
29	REVISED TO ADD...	5/07/69	J. W. B.	
30	REVISED TO ADD...	5/14/69	J. W. B.	
31	REVISED TO ADD...	5/21/69	J. W. B.	
32	REVISED TO ADD...	5/28/69	J. W. B.	
33	REVISED TO ADD...	6/04/69	J. W. B.	
34	REVISED TO ADD...	6/11/69	J. W. B.	
35	REVISED TO ADD...	6/18/69	J. W. B.	
36	REVISED TO ADD...	6/25/69	J. W. B.	
37	REVISED TO ADD...	7/02/69	J. W. B.	
38	REVISED TO ADD...	7/09/69	J. W. B.	
39	REVISED TO ADD...	7/16/69	J. W. B.	
40	REVISED TO ADD...	7/23/69	J. W. B.	
41	REVISED TO ADD...	7/30/69	J. W. B.	
42	REVISED TO ADD...	8/06/69	J. W. B.	
43	REVISED TO ADD...	8/13/69	J. W. B.	
44	REVISED TO ADD...	8/20/69	J. W. B.	
45	REVISED TO ADD...	8/27/69	J. W. B.	
46	REVISED TO ADD...	9/03/69	J. W. B.	
47	REVISED TO ADD...	9/10/69	J. W. B.	
48	REVISED TO ADD...	9/17/69	J. W. B.	
49	REVISED TO ADD...	9/24/69	J. W. B.	
50	REVISED TO ADD...	10/01/69	J. W. B.	

LAST USED NOT USED  
 U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26 U27 U28 U29 U30 U31 U32 U33 U34 U35 U36 U37 U38 U39 U40 U41 U42 U43 U44 U45 U46 U47 U48 U49 U50 U51 U52 U53 U54 U55 U56 U57 U58 U59 U60 U61 U62 U63 U64 U65 U66 U67 U68 U69 U70 U71 U72 U73 U74 U75 U76 U77 U78 U79 U80 U81 U82 U83 U84 U85 U86 U87 U88 U89 U90 U91 U92 U93 U94 U95 U96 U97 U98 U99 U100



NOTE: ALL COMPONENTS SHOWN ARE TO BE USED UNLESS OTHERWISE SPECIFIED.  
 ALL CONNECTIONS MUST BE MADE TO THE TERMINALS.

SALES MARK  
 CONTROL  
 PRICE \$1.00  
 050-3006 E



NOTE: 1. ALL COMPONENT VALUES ARE IN OHMS, UNLESS STATED OTHERWISE.  
 2. ALL FUNCTION VALUES ARE IN MICROSECONDS.  
 3. ALL RESISTOR VALUE UNITS ARE IN OHMS.

16-BIT PARALLEL ADDER-SUBTRACTOR  
 SCHEMATIC  
 16-BIT PARALLEL ADDER-SUBTRACTOR  
 SCHEMATIC

SCHEMATIC  
 16-BIT PARALLEL  
 ADDER-SUBTRACTOR  
 16-BIT PARALLEL  
 ADDER-SUBTRACTOR  
 SCHEMATIC

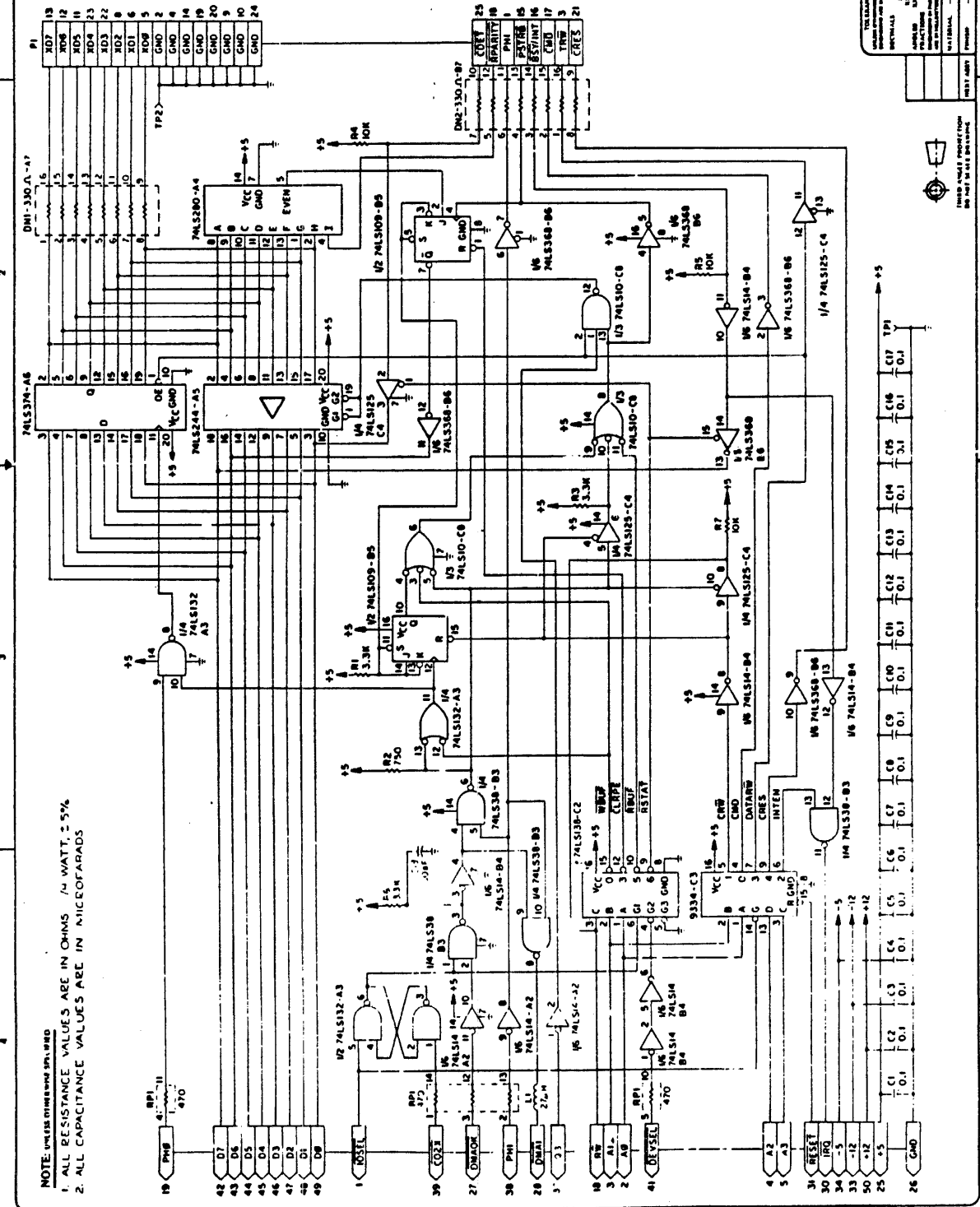


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DATE	050-5737-A
REV	1
BY	W. J. ...
CHKD	...
APPROVED	...
TITLE	SCHEMATIC APPLE II INTERFACE PROFILE
PROJECT	050-5737-A
DESIGNER	...
DATE	...
BY	...
CHKD	...
APPROVED	...
DATE	...
BY	...
CHKD	...
APPROVED	...



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1. ALL RESISTANCE VALUES ARE IN OHMS 1/4 WATT, ± 5%  
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS



74LS132-A1

### Example of Damaged Areas within a Track

As described in the Pro-File HDA Format, page 3.11, sector marks divide each track into 16 separate sectors. The Controller PCB expects the sectors to be in a certain location with respect to the sector marks.

The upper photo shown at the left shows an entire track of data between the two arrows with missing sector marks and other abnormal areas (TPl).

The damaged track was quickly found by using the Big Debugger program to scan from track 0 to park position, (type the command <R +T PE X>, refer to the Big Debugger description in section 2 if more instruction is needed).

The Debugger program stopped the heads at this track when it detected a read error. By looking at the signal at TPl, some abnormalities were seen.

The lower photo shows a enlarged view of a portion of the track in the upper photo. The arrow points to where a sector mark has been written over.

This kind of signal pattern is another probable characteristic of a system Z8 failure. The sector mark was written over and the data put down in such a way so that it could not be read again.

Once the sector mark information is damaged in this way, there is no possible way for the Pro-File to rewrite the sector mark without reformatting.

The diagnostics internal to the Pro-File would probably spare this area under normal circumstances. The HDA must be reformatted to establish the normal sector information (however, this will destroy any data).

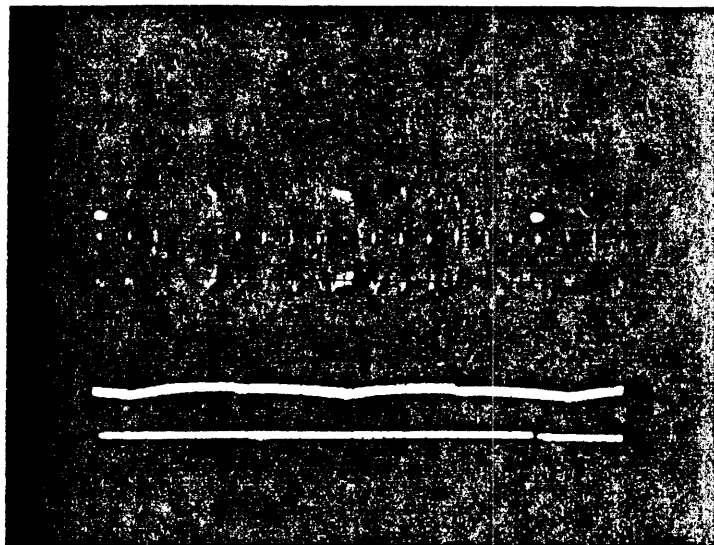
During a scan after powering on, the interrupter stopped momentarily at this track location while the Z8 made attempts to read the damaged sectors.

The sectors on this track were not present in the spares table bad sector list after running the Quick Debugger program.

In a case such as this the only way to continuously find and read the faulty track is to run the Big Debugger program and have it pause on any error. At that point, look at the signal and try to determine the problem.

# Diagnostic Procedure

## Example of Damaged Data Areas on Track



TP1 displays a view of a track of data. There are missing sector marks and other strange areas on the track.

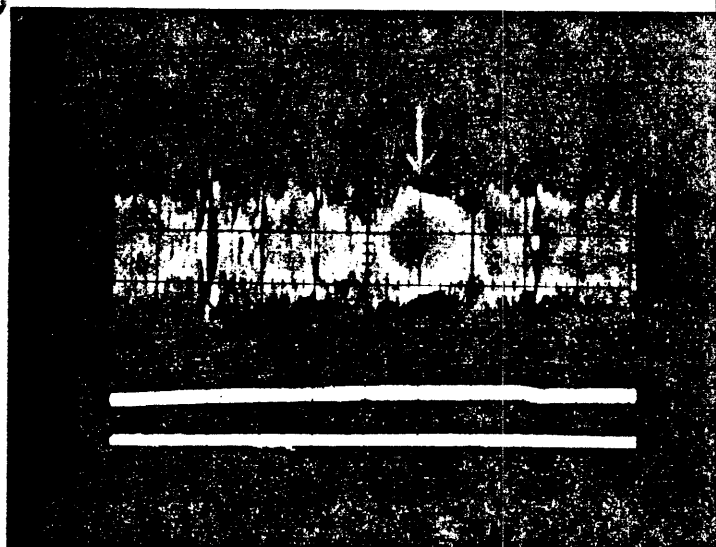
TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div



TP1 displays a closer look at one of the areas of the damaged track. The arrow points to where a sector mark is missing.

TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: .5 msec/div

### Suspect:

1. System Z8
2. Controller PCB
3. HDA

### Example of Damaged Track and Sectors

The upper photo shown at the left shows a partial track of data with one normal sector occurring in the center of the photo.

The other sectors have what appears to be an extra sector mark written in the middle. Not only is the extra sector mark in the wrong position, the width of the sector mark is about three times normal.

The Z8 became confused when reading this sector because of the extra sector marks.

The lower photo shows another track on the HDA with a similar problem (an extra apparent sector mark).

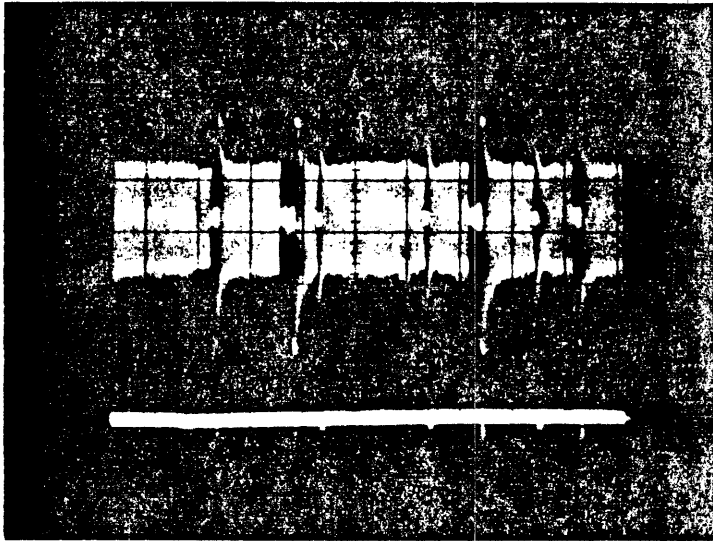
At this point, one should normally suspect the system Z8 as the cause of the damaged sectors.

The problem Pro-File originally had a piggyback system Z8 installed, so there was a very good chance that the Z8 would be the problem.

The Pro-File PCBs were upgraded and the HDA reformatted normally. A 15 minute FST run produced no errors, so the test was continued for 48 hours. No errors occurred.

(except an occasional read error - 08 00 00 00; refer to page 2.37 for a list of errors and how many of a type are acceptable)

# Diagnostic Procedure



## Example of a Damaged Track and Sectors

TP1 displays a partial view of a track of data. There is one normal sector of data shown by the arrow. The other sectors have been overwritten with an abnormal pulse in various places.

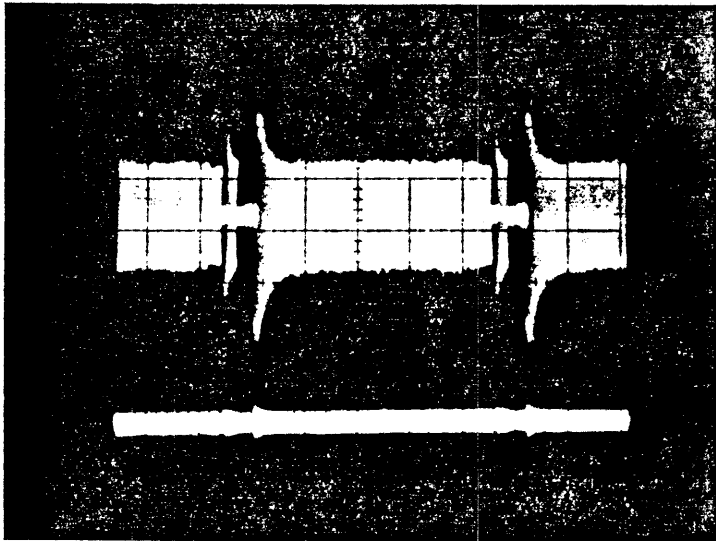
TP8 (VCO) could not lock to the abnormal sectors.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: .5 msec/div



TP1 displays a larger view of the damaged sector.

TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: .2 msec/div

### Suspect:

1. System Z8
2. Controller PCB

### Example of Cleared Data Areas on Track

The upper photo shown at the left shows an entire track of data between the two arrows with about 1/4 of the track damaged.

The sectors in the damaged area have been cleared to a continuous level AC signal by some unknown source, probably the system Z8. Both the sector marks and data areas are missing.

The lower photo shows another track on the same HDA which has been cleared completely of any data and sector marks.

Each signal displays a condition where the HDA wrote a continuous AC signal without using the sector marks as an indicator of where to write.

There is no way for the Pro-File to repair the damaged areas without the technician reformatting the HDA.

Chances are very good that the system Z8 functioned abnormally and caused the Pro-File to write over the data signal; so this would be a good choice for the bad module.

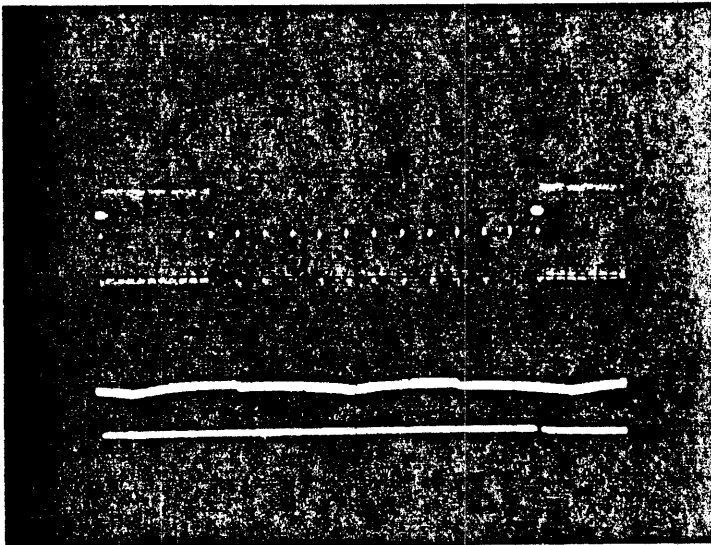
It is also possible that the Controller or Analog PCB could be the cause of the problem because there could have been a short which may have caused the write circuit to malfunction.

For example, a DC voltage shorted to one of the disc heads on the HDA, while the heads were positioned over a track might cause the head to perform a DC erase of the entire track.

This kind of erase would only take about 17 milliseconds to happen (one disc revolution). But if this happened, the signal would be a low amplitude signal, much like a continuous sector mark, etc.

# Diagnostic Procedure

## Example of Cleared Data Areas on Track



TP1 displays a view of a track of data. About a 1/4 of the track has been wiped to a constant AC signal. There are no signs of data in this area.

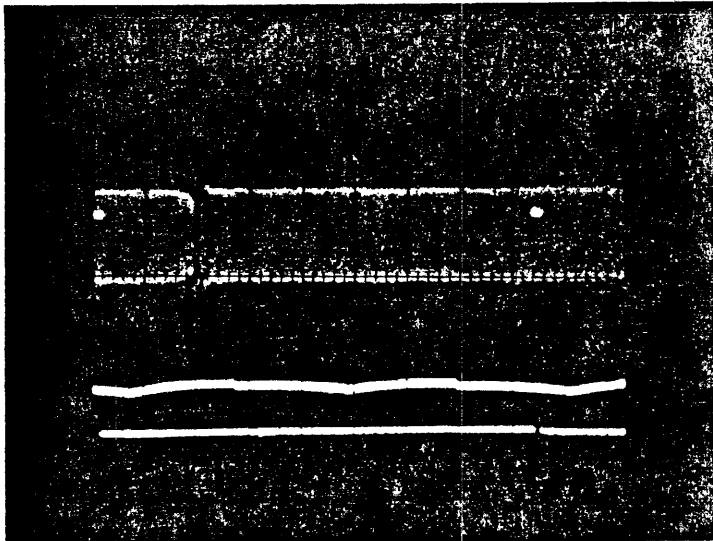
TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div



TP1 displays another track which has been completely cleared of any data except for one small disturbance. An normal track would be between the arrows.

TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div

### Suspect:

- |                   |               |
|-------------------|---------------|
| 1. System Z8      | 3. Analog PCB |
| 2. Controller PCB | 4. HDA        |

### Example of Cleared Data Areas on Track

The upper photo shown at the left shows an entire track of data between the two arrows with about 1/4 of the track damaged.

The sectors in the damaged area have been cleared to a continuous level AC signal by some unknown source, probably the system Z8. Both the sector marks and data areas are missing.

The lower photo shows another track on the same HDA which has been cleared completely of any data and sector marks.

Each signal displays a condition where the HDA wrote a continuous AC signal without using the sector marks as an indicator of where to write.

There is no way for the Pro-File to repair the damaged areas without the technician reformatting the HDA.

Chances are very good that the system Z8 functioned abnormally and caused the Pro-File to write over the data signal; so this would be a good choice for the bad module.

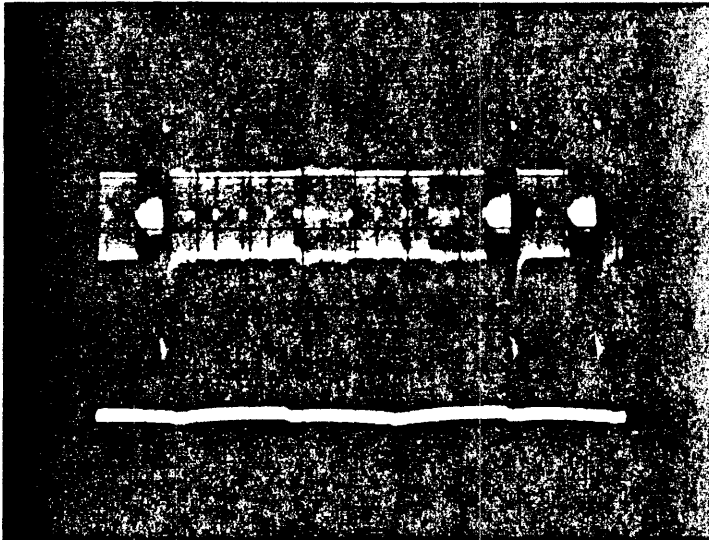
It is also possible that the Controller or Analog PCB could be the cause of the problem because there could have been a short which may have caused the write circuit to malfunction.

For example, a DC voltage shorted to one of the disc heads on the HDA, while the heads were positioned over a track might cause the head to perform a DC erase of the entire track.

This kind of erase would only take about 17 milliseconds to happen (one disc revolution). But if this happened, the signal would be a low amplitude signal, much like a continuous sector mark, etc.



## Diagnostic Procedure



### Example of Offtrack Signal

TP1 displays a view of a track of data. There are 3 sectors which have been damaged.

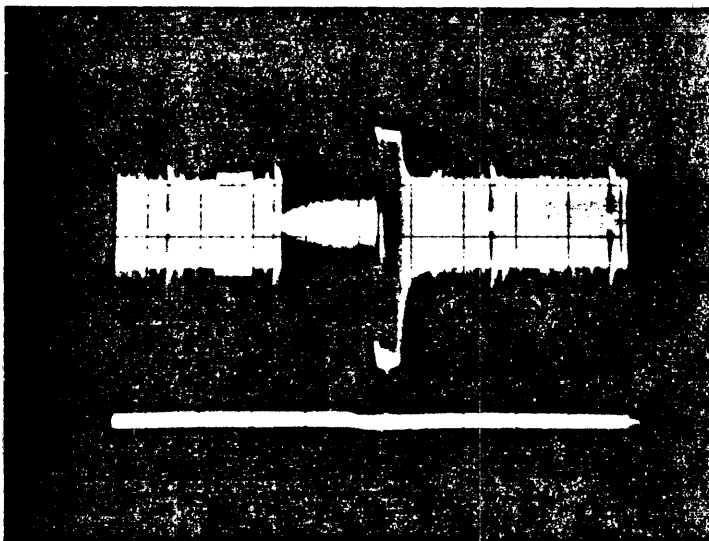
TP8 (VCO) was not able to lock on to this kind of abnormal data signal at TP1

#### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div



TP1 displays a closer view of some of the sectors of the track, including the bad area. The signal shows that two sectors have actually been damaged.

TP8 (VCO) is not used here.

#### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: .5 msec/div

#### Suspect:

1. System Z8
2. Controller PCB
3. HDA

## Example of Offtrack Signal

As described in the physical description of the Pro-File HDA format in section 3 of this manual, the data areas are written on the disc surfaces in tracks, and the Z8 performs the Seek routine to cause the stepper motor to move the heads over the target track to access data. The number of step pulses the Z8 sends to the stepper motor determines how far the head will move and so which track it will be over. (For an explanation of the Seek routine refer to the Firmware Routines description in section 3.) Because the control system is of open loop nature, (i.e. there is little feedback telling the Controller PCB where the disc heads are physically located) both mechanical and electronic offtrack problems can occur.

A mechanical offtrack problem within the HDA can be caused by several things. The stepper motor controlling the position of the heads can become inaccurate placing the heads slightly offtrack either way. The metal band which pulls the heads back and forth can become torn or damaged resulting in poor placement of the heads. The mechanical assembly holding the bearings for the movement of the heads can become distorted causing every track to be shifted one way. Or the HDA stepper motor could have a hysteresis problem. Any of these problems can only be corrected by replacing the HDA.

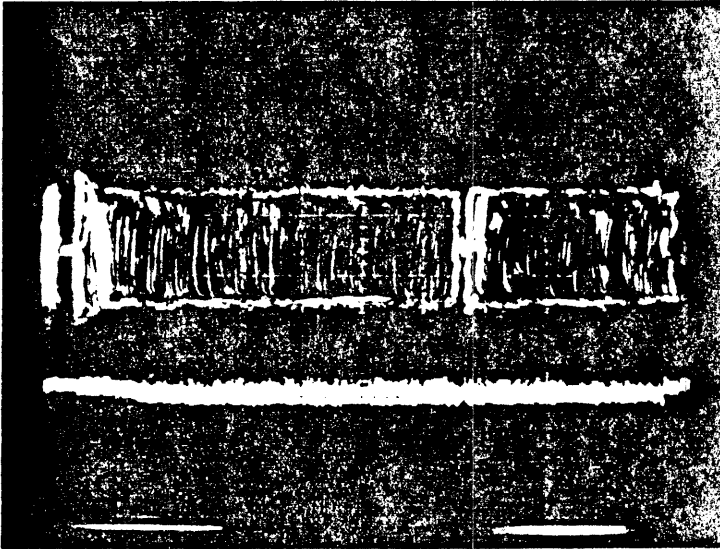
An electronic problem can resemble that of a mechanical one, except that there is generally no permanent damage done to the HDA. After reformatting, the HDA can be returned to normal service, as long as the problem has been eliminated from the system. If the system Z8 was an older revision piggyback type, then it is probably the bad component. This is because the Z8 has historically been the most common failed component in the Pro-File.

Another electronic failure that can cause an offtrack problem is the Controller PCB.

The upper photo shows three sectors which have been damaged by the system Z8 microprocessor by writing the data in an offtrack position. The lower photo shows a closeup of the analog signal where two sectors have actually been damaged. By telling the system to attempt to read the sector continuously, and carefully and gently moving the interrupter arm towards the target track, the signal became normal. This confirmed the fact that the sectors were written offtrack. By replacing the piggyback system Z8 with a masked ROM version, reformatting the HDA the problem disappeared. This was confirmed by running the Pro-File on FST for 48 hours.

# Diagnostic Procedure

## Example of Bad Media



TP1

TP1 displays a closer view of a suspected bad area of a track. In about the middle of the sector there appears to be a section missing some magnetic material.

TP8

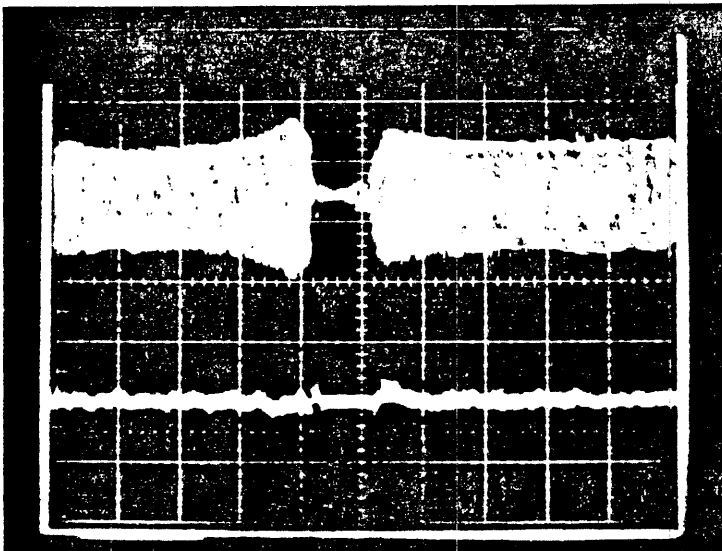
TP8 (VCO) does not show any particular abnormality.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: .1 msec/div



TP1

TP1 - displays a larger view of the sector shown above. On closer examination, the dead area appears as a sector mark, except much smaller in width.

TP8

TP8 (VCO) displays as flat signal, as it would between normal sector marks

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: .01 msec/div

### Suspect:

1. Media Problem

## Example of Bad Media

Bad Media is an example of where the HDA disk surface coating has been damaged by either a defect in the magnetic coating or a scratch due to head contact with the media. There are a limited number of allowable defects per disk surface. These defects (hard errors) are defined as  $\leq 2$  bytes in length. The total number of defects is:

Per Drive	32 errors total
Per Surface	8 errors total
Track 0	No errors allowed

The HDA disk drive uses two double sided 5-1/4 inch discs coated with an iron oxide base material as the recording media. The disc dimensions are 40mm inside diameter and 130 mm outside diameter. The thickness of the magnetic coating increases linearly from 20 microinches to 40 microinches at the outside diameter. The disk surface is coated with a Teflon lubricant 40 to 60 angstroms in thickness. (an angstrom = 0.000000004 inches)

The media defect shown at left was detected by looking at the spares list of supposedly bad sectors, created by the Quick Debugger program and then telling the Big Debugger program to continuously read the suspect sector.

An initial view of the track looked completely normal, except for the fact that one of the sectors produced an error when reading.

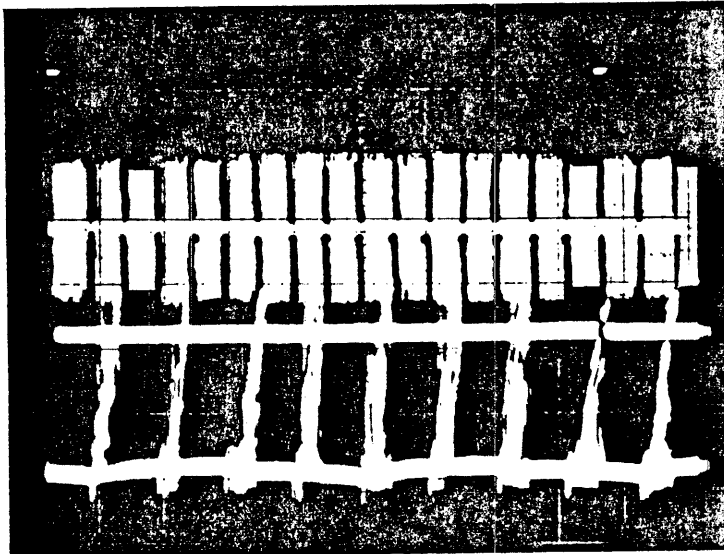
By displaying the whole sector, there appeared to be a small area of no signal present (Refer to upper photo). Closer examination (by using the delay trigger function of the oscilloscope) of the suspect area of the sector, shows a total loss of signal in this area (lower photo).

If bad media is suspected an attempt should be made to write data to the sector(s) in question before the conclusion can be made that the suspect area is actually a media problem.

The Big Debugger allows the technician to read a sector into the computer buffer and write the sector back out to the 'bad' sector on the Pro-File. (Refer to page 2.40, for instructions on the Big Debugger program. Use the command <W> to write.)

If the number of total errors incurred by reading the media is greater than or equal to the total number of errors shown above, then the HDA should be rejected as defective.

# Diagnostic Procedure

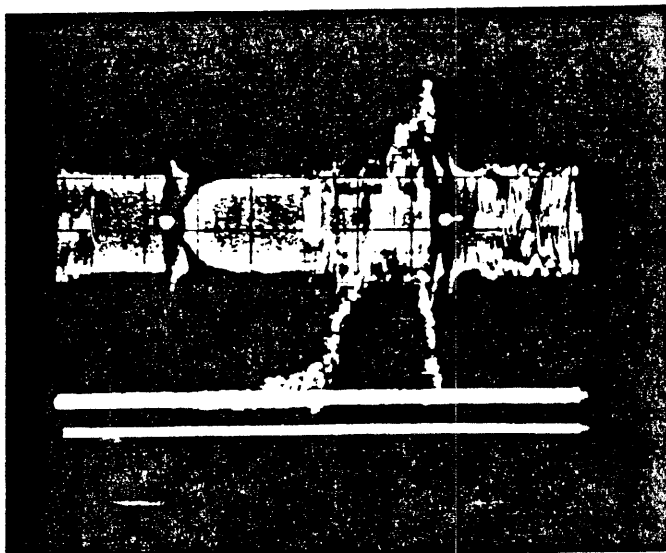


Example of Abnormal VCO Signal at TP8

TP1 displays a view of a track of data. (The entire track appears between the two arrows)

TP1 TP8 (VCO) displays a very high amplitude signal (2v). This abnormal voltage is due to the errors occurring when reading.

TP8 Scope Settings:  
TP1 - 1 volt/div  
TP8 - .5 volt/div  
Timebase: 2 msec/div



TP1 displays a closer view of one of the sectors of a track. This sector (and all others of the track) has been written offtrack.

TP1 TP8 (VCO) tries to correct for the offtrack condition by boosting its amplitude voltage. This effect is seen at the left.

Scope Settings:  
TP1 - 1 volt/div  
TP8 - .5 volt/div  
Timebase: .2 msec/div

Suspect:

1. Analog PCB
2. HDA

### Example of Abnormal VCO charge pump Signal

During a normal read operation, the Pro-File locks to the analog data signal by comparing the phase of the clock in the analog read signal with the phase of the VCO. If the VCO leads or lags the analog data clock a positive or negative correction voltage is stored in the charge pump capacitor. The charge on this capacitor is the voltage controlling the VCO, and can be seen at TP8 on the Analog PCB (usually  $\pm 1$  volt Peak to Peak).

To change the frequency, the Pro-File changes an input voltage to the VCO.

If the VCO charge pump signal (TP8) is observed along with the data signal (TP1) and a large deviation in VCO charge pump voltage appears (similar to the spikes in the upper photo), the VCO circuitry on the Analog PCB could be causing the abnormal VCO charge pump voltage to occur.

By changing the timebase to read a single sector (the lower photo), notice that both the analog data signal at TP1 and the VCO charge pump voltage at TP8 appear abnormal.

TP1 displays an offtrack condition (noted by the pinching of the signal following the sector mark), where the head is not positioned directly over the written data signal.

This offtrack condition can be either caused by an electronic or HDA related failure. (There are more examples of an offtrack data signal earlier in this procedure.)

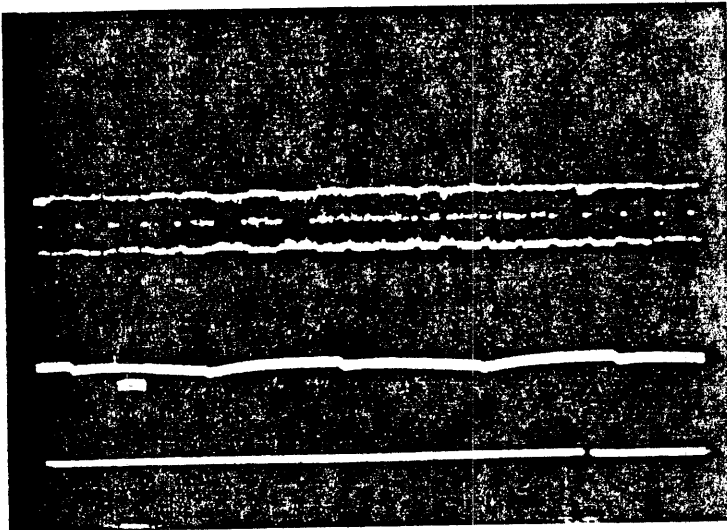
As it turned out, every track on the particular HDA which produced this picture showed an analog data signal similar to TP1 (in the lower photo).

Because every sector of every track on the HDA was offtrack, it might be concluded that the HDA is bad because of the consistency in head misalignment.

The problem could be remedied by reformatting, but this would not be a good thing to do as the reason why the Pro-File went offtrack is not known. (Unknown damage internal to the HDA itself)

# Diagnostic Procedure

Example of Abnormal AGC  
(Automatic Gain Control)



HORZ SWP = 2ms/DIV

TP1 displays a view of a track of data. The track amplitude is about half the expected value of 2 mv p-p.

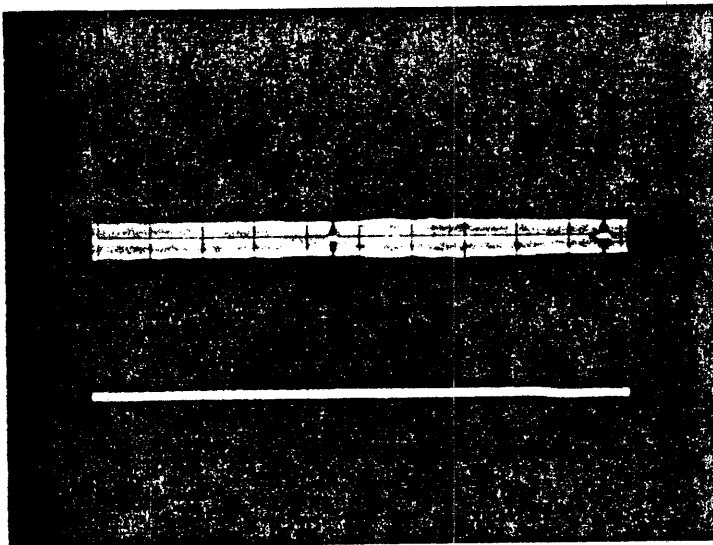
TP8 (VCO) is not used here

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: 2 msec/div



TP1 displays a closer view of some of the sectors of the track. Note that the sectors don't have the bell shape near the sector mark.

TP8 (VCO) is not used here.

### Scope Settings:

TP1 - 1 volt/div

TP8 - .5 volt/div

Timebase: Variable

### Suspect:

1. Analog Card
2. HDA

### Example of Abnormal AGC

A normal data signal read at Test Points 1 & 2 on the Analog PCB have an average amplitude voltage of about 2 volts peak to peak.

If there is a malfunction in the amplifier circuits between the disc heads and TPl & 2, the signal amplitude can be much less. For example, the analog to digital conversion circuits may be able to operate with voltages as low as 1.1 volt Peak to Peak.

Below 1.1 volt the analog circuitry just does not get a large enough amplitude signal to function.

The AGC circuitry was added to overcome normal changes in signal as the head seeks back and forth between the inner and outer tracks.

Decreases in the thickness of media coating or head flying height tend to cancel a loss in signal. Inner tracks will usually have the lowest amplitude signals.

In the upper photo at the left, the AGC circuitry was not functioning correctly as the amplitude was about 1 volt peak to peak.

After power up, the interrupter began to scan normally until about track 100, when the scan stopped.

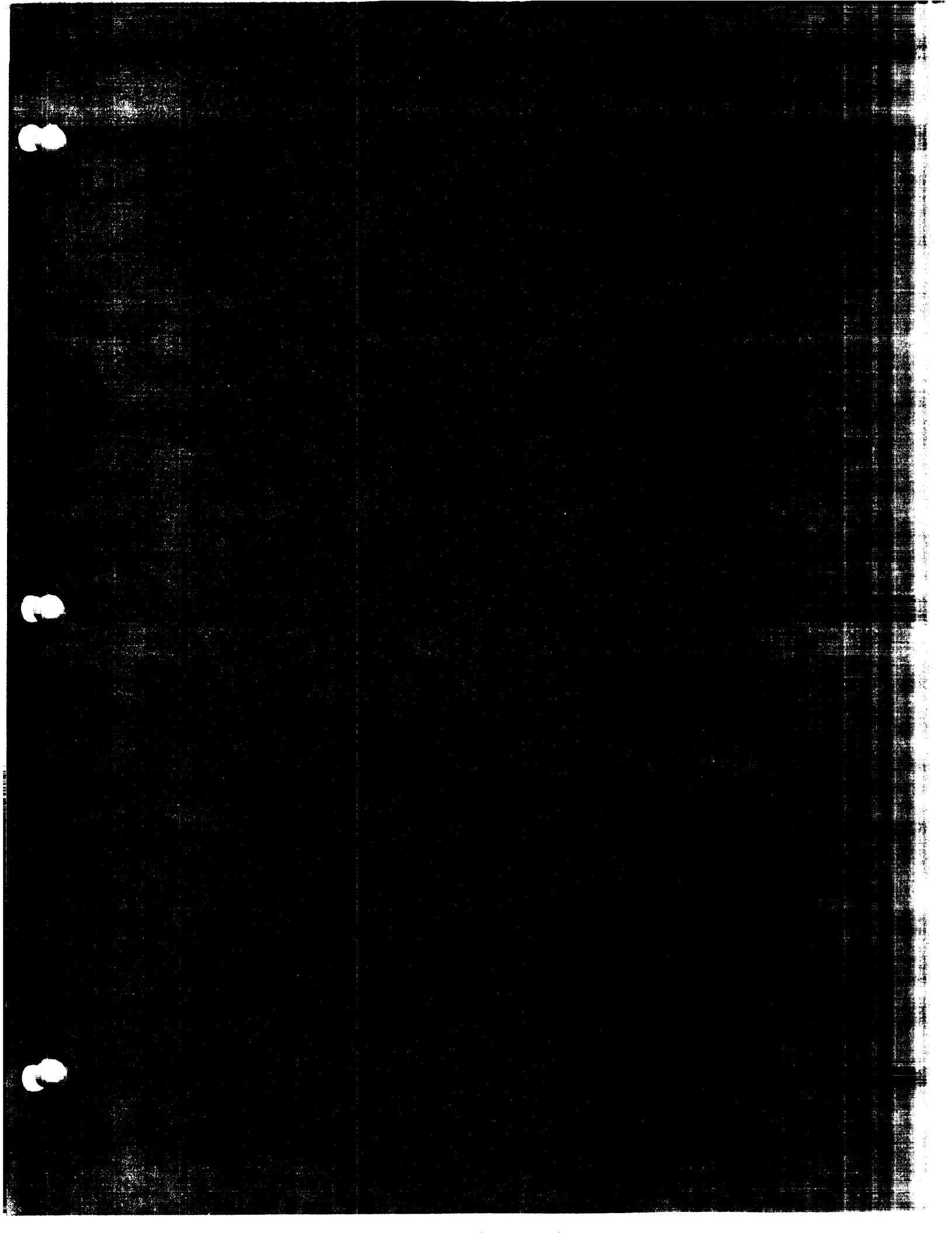
Several hours later the interrupter was still stopped on the same track, unable to read the data present there.

The lower photo shows an expanded view of one entire sector from another track. Note that the normal flared shape present immediately after the sector mark is missing.

This missing "bell" shape is a characteristic of a faulty AGC circuit on the Analog PCB.

The Analog PCB was replaced and the Pro-File functioned normally.





**SECTION 2**  
**SERVICE PROCEDURES**

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#### HOW TO USE THIS SECTION:

This section contains the removal/replacement, check and adjustment, and software operation procedures you will need to repair the Pro-File.

If you are unsure which procedure to perform, go to the troubleshooting procedure in the Troubleshooting Section and follow the directions.

## PROFILE MODULE REMOVAL AND REPLACEMENT PROCEDURES

### INTRODUCTION

The following equipment will be needed in these procedures:

Diagonal cutters ("dikes")	Protective Pad
Tie Wraps	Medium Phillips Screwdriver
Small Flatblade Screwdriver	Needlenose pliers

**CAUTION:** The ProFile is a mechanical device with motors and moving parts. Rough handling such as dropping the drive, sharply jarring it or allowing heavy objects to fall on it can cause a malfunction. Whenever it is necessary to turn the ProFile over, be sure to rest it on a protective pad.

UNDER NO CIRCUMSTANCES SHOULD THE HDA BE ENTERED!

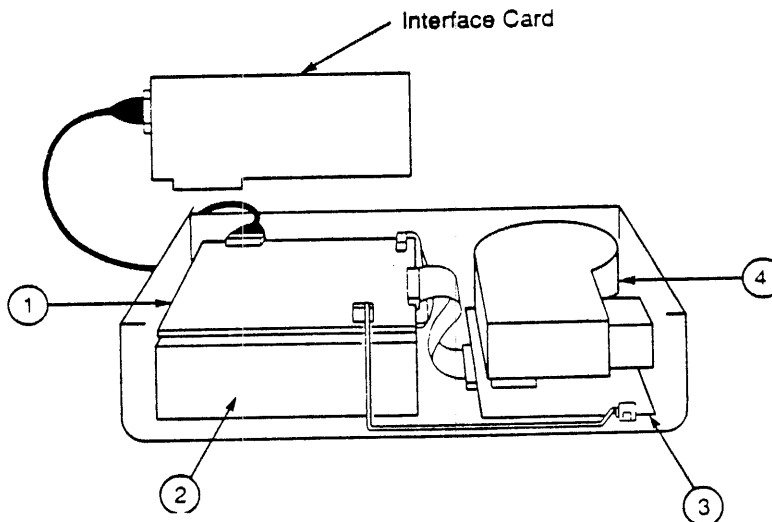


FIGURE 1

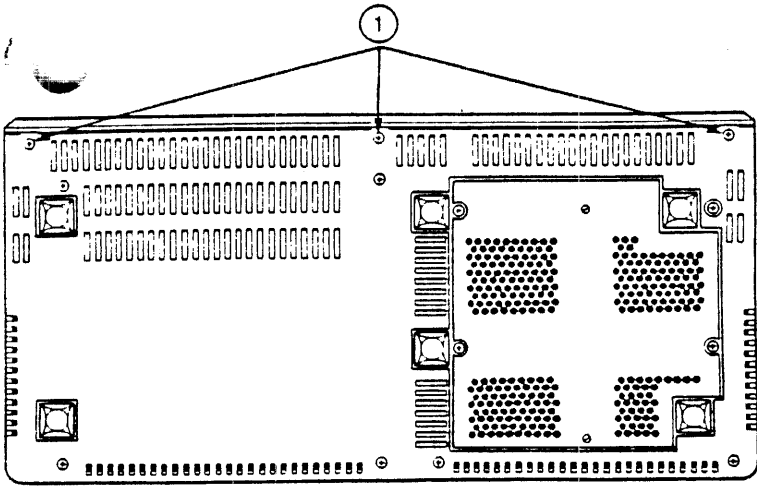


FIGURE 2

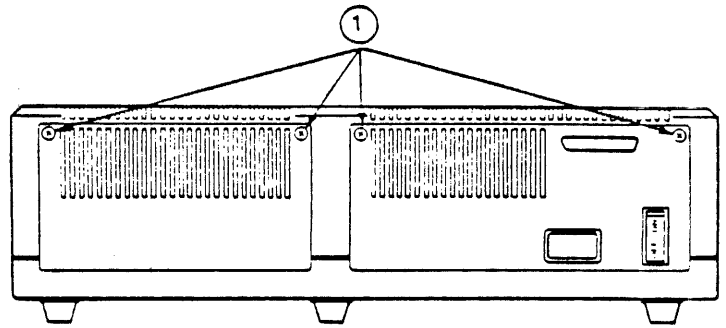


FIGURE 3

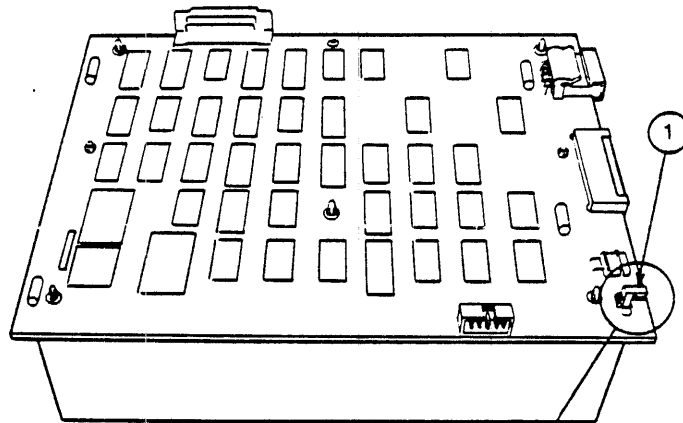


FIGURE 4

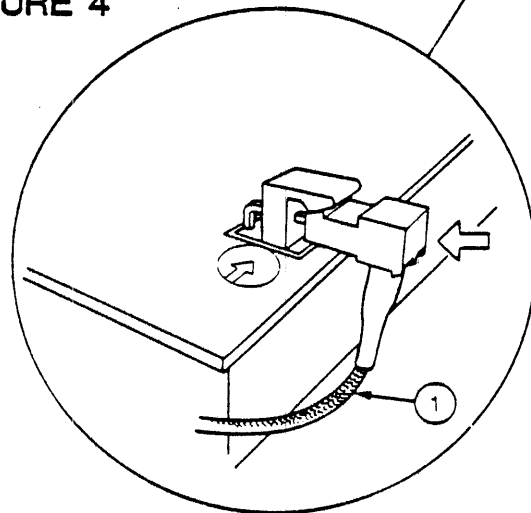


FIGURE 5

## A. THE PRO-FILE COVER

### Removing the Cover:

1. Make sure the ProFile is turned off. Disconnect the power cord and interface cable (ribbon cable) from the back of the ProFile.
2. Turn the ProFile over, lay it on the protective pad, and remove the three Phillips-head screws from beneath the front panel (Figure 2, #1).
3. Turn the ProFile right side up; loosen but do not remove the four screws on the back of the unit (Figure 3, #1).
4. Carefully pull out the lip on the bottom of the cover to disconnect it from the frame.
5. Take care not to pull on the LED cable as you carefully lift the cover off and rest it on the far side of the case, .
6. Unplug the LED cable from its socket on the controller PCB (Figure 4, #1).

### Reinstalling the Cover:

1. Attach the LED cable to its connector on the controller PCB (Figure 5). Make sure the LED cable exits down and away from the PCB (Figure 5, #1).
2. Replace the ProFile cover. (Hints: The four slots on the back of the cover fit between the inner and outer rear plates, over the four loosened screws. Line up the back first; then pull the cover gently forward and down. Check around the cover to make sure the LED cable isn't caught between the cover and the base; then tighten the four rear-plate screws.)
3. Turn the ProFile over and replace the three screws on the front edge (Fig. 2).
4. Turn the ProFile right side up. Reinstall the power cord and the interface cable.

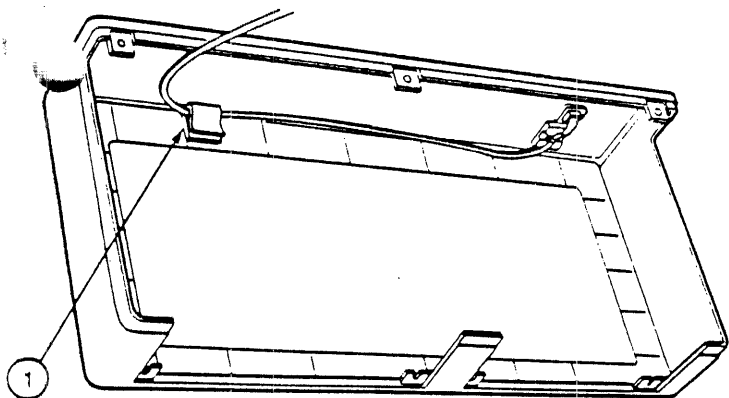


FIGURE 6

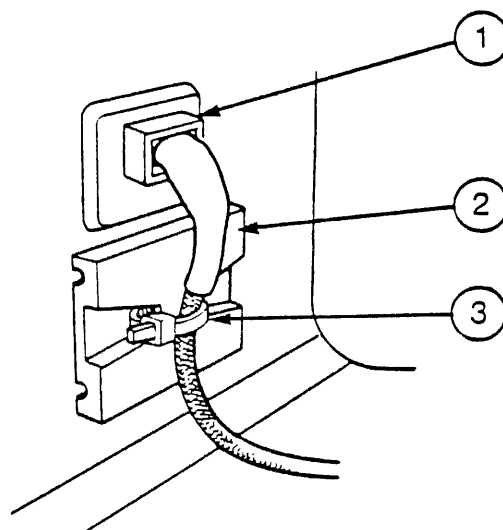


FIGURE 7

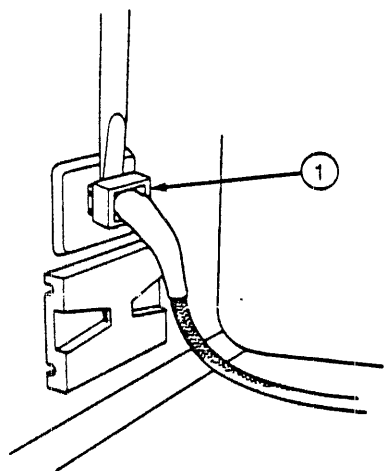


FIGURE 8

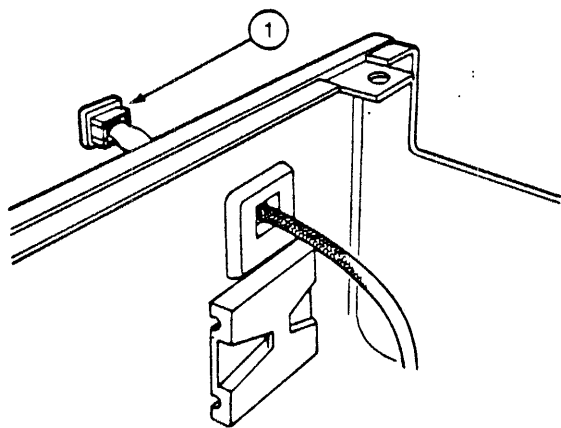
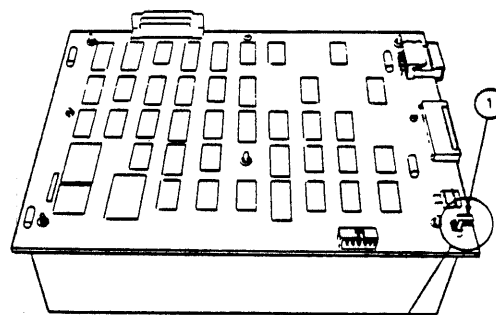


FIGURE 9

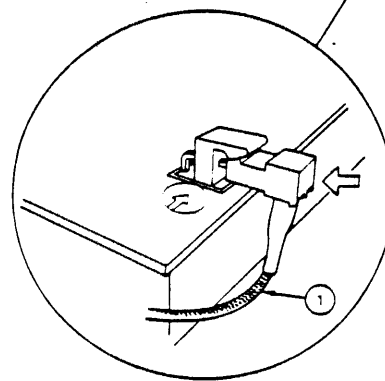


FIGURE 10



## B. THE READY L.E.D.

### Removing Ready LED:

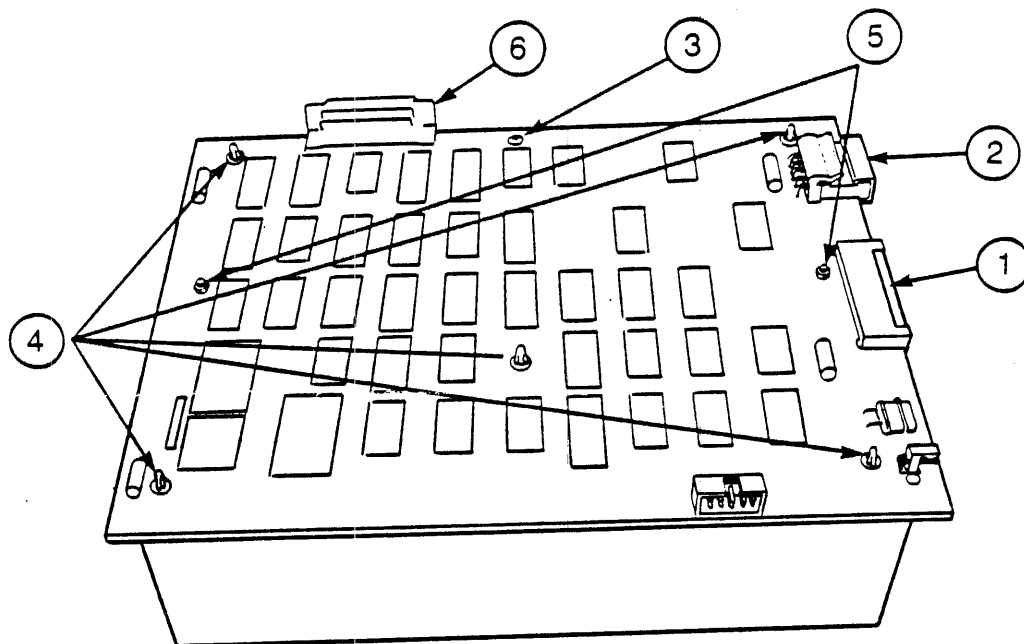
1. Remove the ProFile cover and disconnect the LED cable from the controller PCB. Lay the cover flat, as in Figure 6.
2. Cut off the white plastic tie (Figure 7, #3) that holds the LED cable to the white holder in the cover (Figure 7, #2).
3. Remove the other end of the LED cable from the other holder in the cover. (On some ProFiles, this holder will be a clamp like the one shown in Figure 6, #1; on others, it will be like the one shown in Figure 7.)
4. With a flathead screwdriver, pry the cable clamp off the back of the LED (Figure 8, #1) and slide it down the cable, out of the way.
5. Gently push a few inches of the cable out through the slot in the cover, as shown in Figure 9.

NOTE: You may have to remove the "ready" label around the LED opening on the cover to free the LED.

6. Around the red LED is a small black plastic mount. Remove the mount (Figure 9, #1) by pushing out its side flaps and sliding it off the LED.
7. Pull the cable back through the hole in the case.

### Installing the Ready LED:

8. Thread the LED cable through the opening in the cover, and place the small black plastic mount on the LED (see Figure 9, #1). Then pull the cable back through the opening until the LED fits in its slot. Replace the "ready" label.
9. Push the cable clamp (Figure 7, #1) up to the cover until it holds the cable steady.
10. Place the LED cable against the white plastic holder and fasten it with a tie wrap (Figure 7, #2 and 3).
11. Place the cable in the other holder (Figure 6, #1), using a tie wrap if necessary. Cut off excess tie wrap.
12. Connect the LED cable to the controller PCB (Fig. 10) and reinstall the cover.



**FIGURE 11**

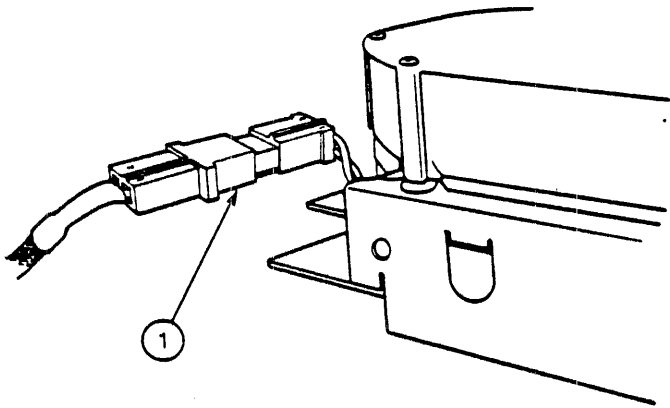
### C. THE CONTROLLER PCB

#### Replacing the Old PCB:

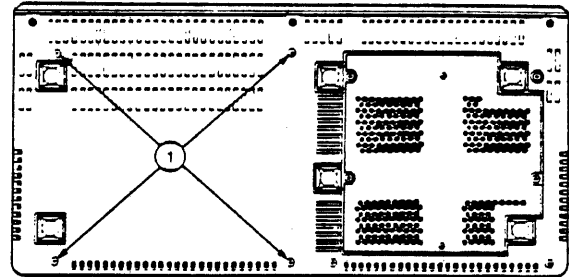
1. Remove the cover and disconnect the LED from the controller PCB.
2. Disconnect the ribbon cable (Figure 11, #1) and (as far as you can) the orange Mylar motor control cable (Figure 11, #2) from the controller PCB. (You can finish disconnecting the motor control cable more easily after taking the PCB out.) NOTE: Do not pull on the ribbon cable (analog-to-controller cable). Push and wiggle the grey plastic connector until it comes free of the PCB.
3. Remove the long screw at the middle rear of the controller PCB (Figure 11, #3).
4. Use the needlenose pliers to push in the flanges of each of the five plastic stand-offs (Figure 11, #4), to release the PCB. NOTE: Some PCBs will have two additional stand-offs, or two screws to remove, as shown in Figure 11, #5.
5. Lift the controller PCB forward and up off the power supply - you may have to push out on the rear plate to free the interface cable connector (Figure 11, #6), and finish disconnecting the motor control cable. Set the PCB aside. NOTE: When you lift off the controller PCB, you will see a loose metal spacer under the spot where you removed the long screw. Save this spacer for use with the new PCB.

#### Installing the New PCB:

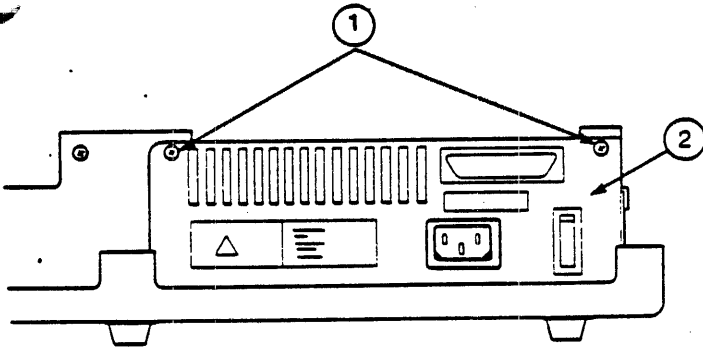
6. Holding the controller PCB over the power supply, position the interface cable connector (Fig. 10, #6) in its slot in the rear plate.
7. Position the controller PCB over the five plastic stand-offs, but don't push it down yet.
8. Connect   a) the orange Mylar motor control cable and  
          b) the analog-to-controller ribbon cable.
9. Slide the metal spacer under the PCB so that it is underneath the rear, middle screw hole. Insert the long screw through the hole and the spacer without tightening it.
10. Gently push the PCB down until the stand-offs hold it firmly in place; then tighten the long screw.
11. Connect the LED cable and replace the cover.



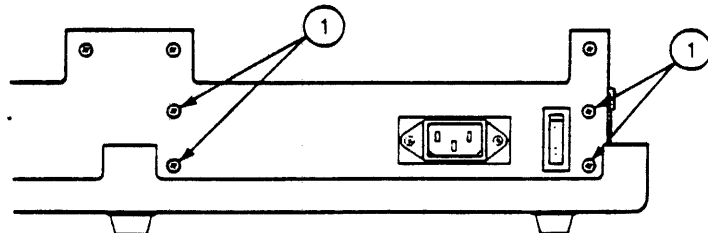
**FIGURE 12**



**FIGURE 13**



**FIGURE 14**



**FIGURE 15**

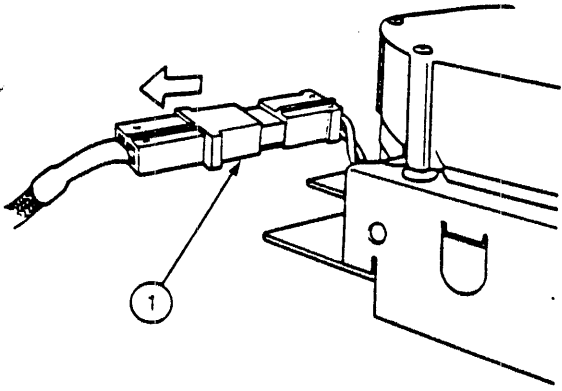
## **D. THE POWER SUPPLY**

### **Removing the Old Power Supply**

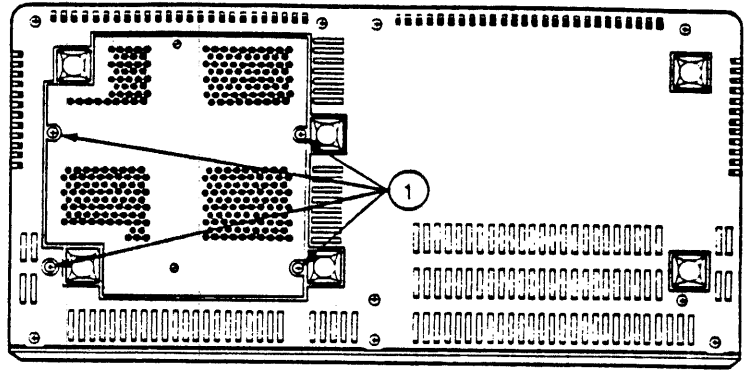
1. Remove the cover, disconnect the LED cable and remove the controller PCB.
2. Disconnect the small white power supply plug (between the power supply and the HDA) from its mate (Figure 12, #1).
3. Turn the ProFile over and rest it on a foam pad. Remove the four screws that hold the power supply onto the bottom of the ProFile case (Figure 13, #1).
4. Hold the power supply in place as you turn the ProFile right side up. Position it with its rear plates facing you. Find the longer of the two rear plates, remove the two screws that hold it on (Figure 14, #1), and remove the plate (Figure 14, #2).
5. Remove the four screws that hold the power supply to the inner rear plate (Figure 15, #1), and lift out the power supply.

### **Installing the New Power Supply**

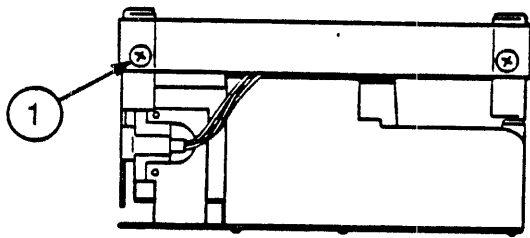
1. Position the power supply unit in the ProFile frame so that the two cables come out toward the HDA. Line up the four screw holes in the back of the power supply with the four lower holes in the inner rear plate; install the four screws.
2. Replace the outer rear plate. Insert the two mounting screws that hold this plate to the inner rear plate, but don't tighten them all the way.
3. Connect the two-pronged power supply cable to its mate from the HDA (Figure 12, #1); reconnect them behind the orange Mylar cable (i.e., closer to the HDA).
4. Holding the power supply in place, turn the ProFile over onto the workpad. Replace the four screws that hold the power supply to the bottom of the case. Turn the ProFile right side up.
5. Reinstall the controller PCB.
6. Connect the LED cable to the controller PCB and put the ProFile cover back on.



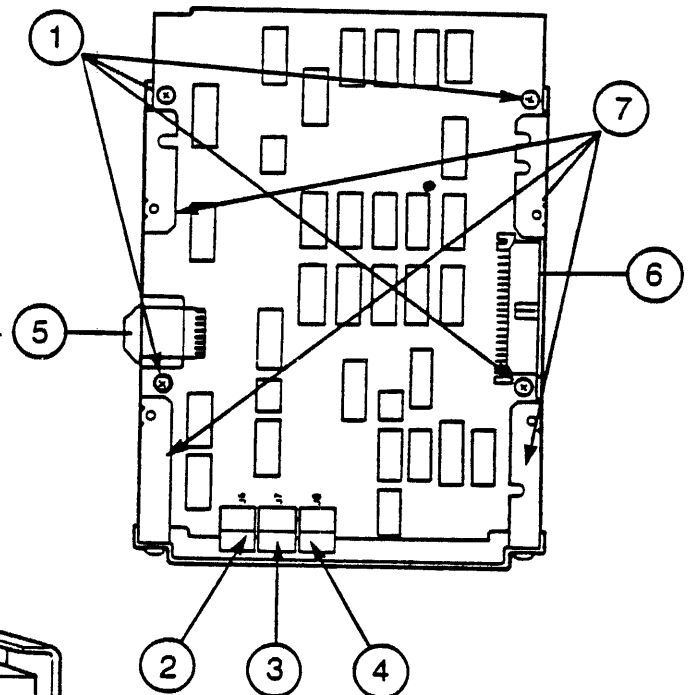
**FIGURE 16**



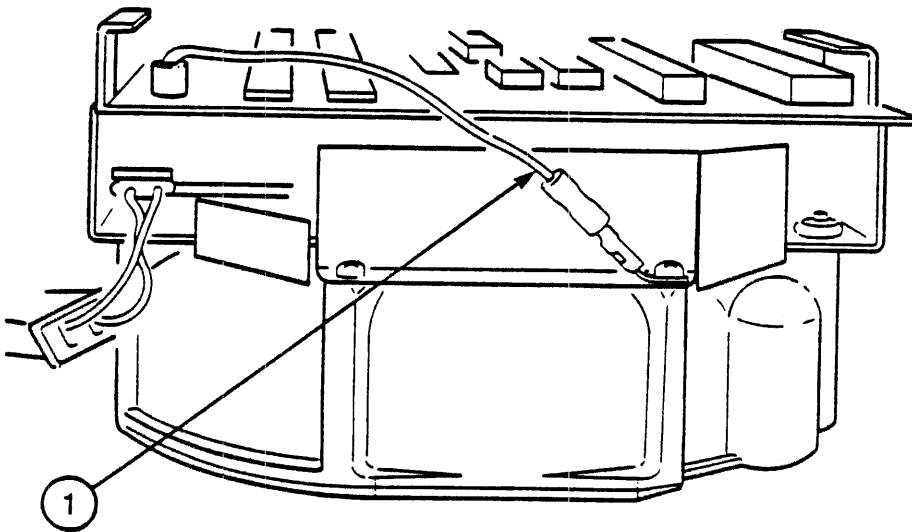
**FIGURE 17**



**FIGURE 18**



**FIGURE 19**



**FIGURE 20**

## E. THE HARD DISK ASSEMBLY (HDA), AND ANALOG PCB

### Removing the Old HDA and Analog PCB:

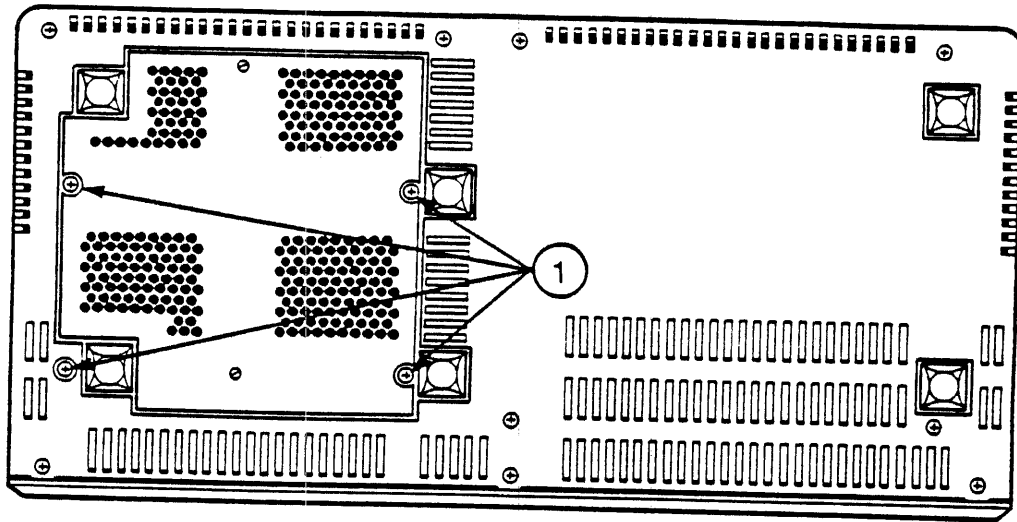
1. Remove the cover, disconnect the LED cable, and disconnect the cables that connect the HDA to the power supply and controller PCB.
2. Turn the ProFile over and rest it on the protective pad. Remove the four screws that mount the HDA to the ProFile housing (Figure 15, #1).
3. Carefully lift the housing up and off. Keep the HDA on the protective pad.

### Removing Old the Analog PCB:

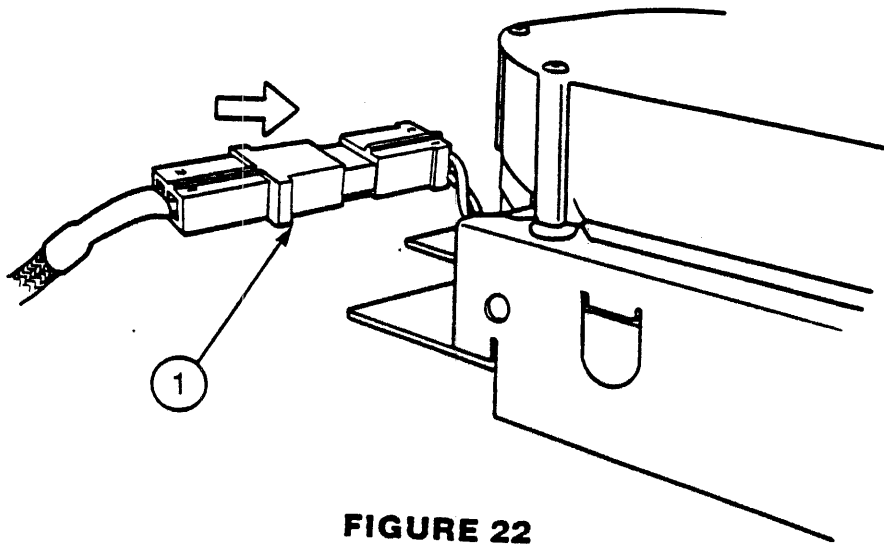
1. Turn the HDA so that the ribbon cable comes out to your right.
2. If there is a metal bar across the front of the analog PCB as shown in Figure 16, #1, or over the top of the analog PCB, remove the screws that hold the bar in place and set the bar aside. NOTE: This bar does not exist on later models.
3. Three small cables (Figure 17, #2, 3, 4) connect to one side of the PCB. The plug and socket of each cable should bear a corresponding number, so that you can tell which plug goes in which socket. If such numbers are not present, write them in with a marker.
4. Carefully disconnect all five cables from the analog PCB:
  1. Index cable (Figure 17, #2)
  2. Stepper motor cable (Figure 17, #3)
  3. Track 0 cable (Figure 17, #4)
  4. Head cable (Figure 17, #5)
  5. Analog-to-controller cable (Figure 17, #6)
5. Turn the HDA so that the rounded side is facing you, and remove the ground strap (Figure 18, #1) by grasping its plug firmly with the needlenose pliers and pulling.

**CAUTION:** This is a short wire and its connection is tight. Use minimum force to prevent ripping it off the analog PCB.

6. Remove the four Phillips-head mounting screws from the analog PCB (Figure 17, #1).
7. Gently squeeze outward on the rails (Figure 17, #7) and lift the analog PCB from the HDA.



**FIGURE 21**



**FIGURE 22**



### **Installing the New Analog PCB:**

8. Slide the analog PCB back under the rails. Line up the holes in the PCB with the screw holes on the rail.
9. Reconnect the analog-to-controller (ribbon) cable. (Do not use the arrow on the ribbon cable connector as a guide to connecting it. The ribbon cable should exit down and away from the analog PCB, and the side of the connector where the ribbon cable curls over a bar should be on top.)
10. Reconnect the other four cables. Check to make sure they are connected to the right plugs.
11. Replace the four Phillips-head mounting screws in the analog PCB.
12. Reconnect the ground strap.
13. If there was a metal bar over the rail, replace it and reinstall its screws.
14. Reinstall the HDA, reconnect all cables, and replace the cover.

### **Reinstalling the HDA:**

1. Turn the HDA so that the ribbon cable comes out to your right.
2. Place the ProFile case over the analog PCB (see Figure 19: the rear plates of the case should be on the far side of the HDA). Line up the screw holes in the case with the screw holes in the railings over the analog PCB (Figure 19, #1).
3. Reinstall the screws.
4. Turn the ProFile right-side up, with the rear plate facing you. (The ribbon cable should now extend out from the bottom of the HDA.)

J2 ON THE OLD MOTOR  
CONTROL PCB, LEADS  
TO THE BRAKE

### OLD MOTOR CONTROL PCB

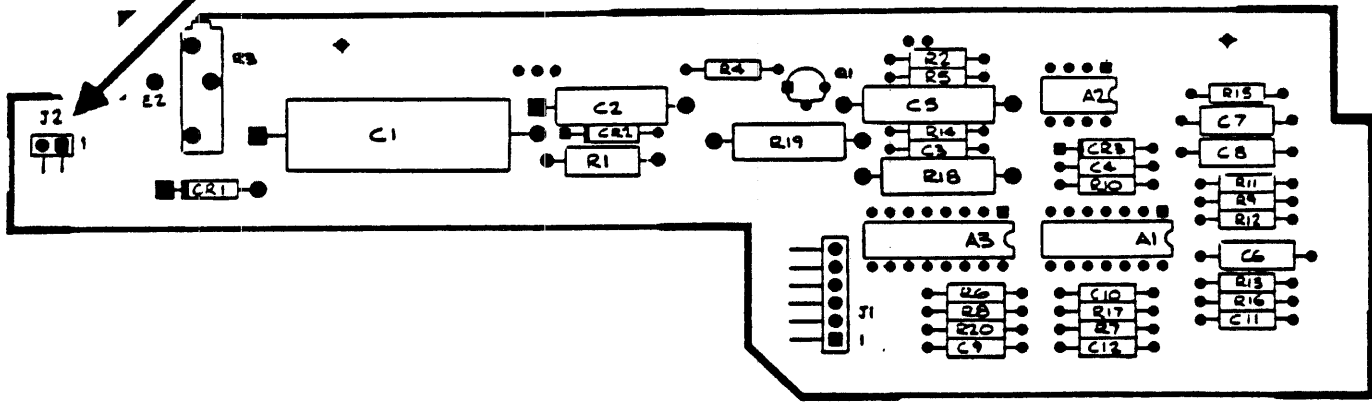
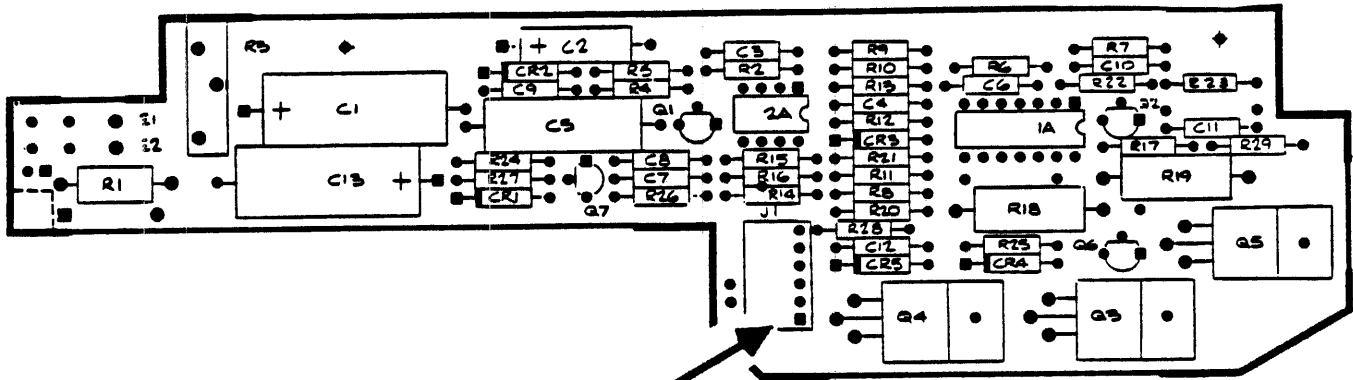


FIGURE 1

### NEW MOTOR CONTROL PCB



ON THE NEW MOTOR  
CONTROL PCB,  
PIN 1 ON THE MOLEX  
PLUG IS AN EXTRA PIN

FIGURE 2

## F. THE MOTOR CONTROL PCB

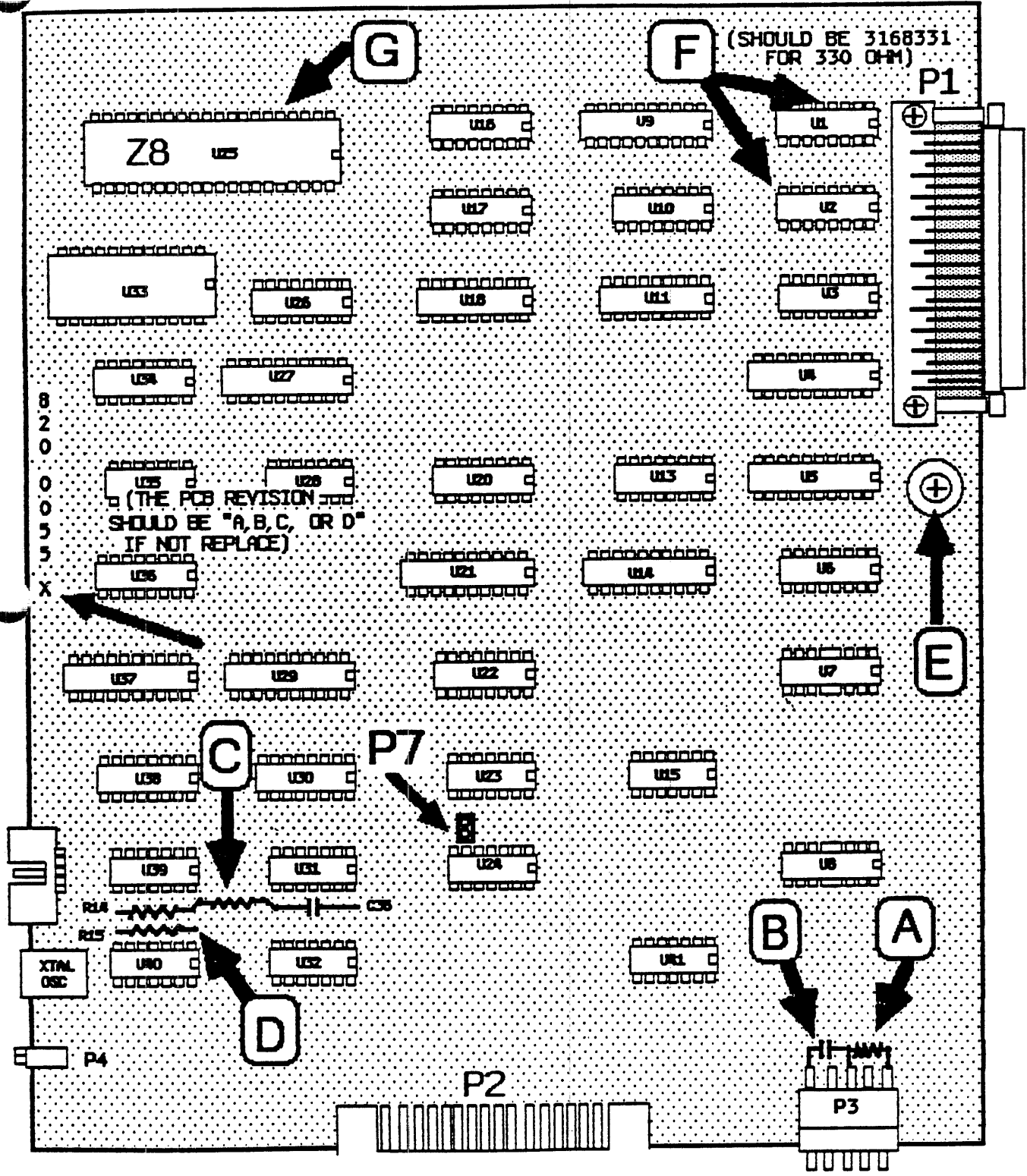
1. Remove the HDA and the Analog PCB as described in the HDA and Analog PCB Removal/Replacement procedure found in this section.
2. Refer to the illustrations on the opposite page to identify whether you have an old or new Motor control PCB. Your replacement motor control PCB should always be a new revision.

\*\*\* If you have an old motor control PCB, then you must remove the brake on the HDA in addition to removing the motor control PCB.

\*\*\* If you have a new motor control PCB then P1 may be a 7 pin Molex plug fitting on J1 a 6 pin jack. In this case pin 1 on the plug will be the extra pin with pins 2 through 7 of the plug fitting onto pins 1 through 6 of the jack.

3. Remove the motor control PCB by disconnecting all plugs, and removing the 2 screws fastening it to the HDA main assembly.
4. Reinstall the motor control PCB by reconnecting the plugs, and reinstalling the 2 screws to fasten the PCB to the HDA main assembly.

# CONTROLLER PCB



## CONTROLLER BOARD UPGRADE PROCEDURE

The following equipment may be needed for this procedure:

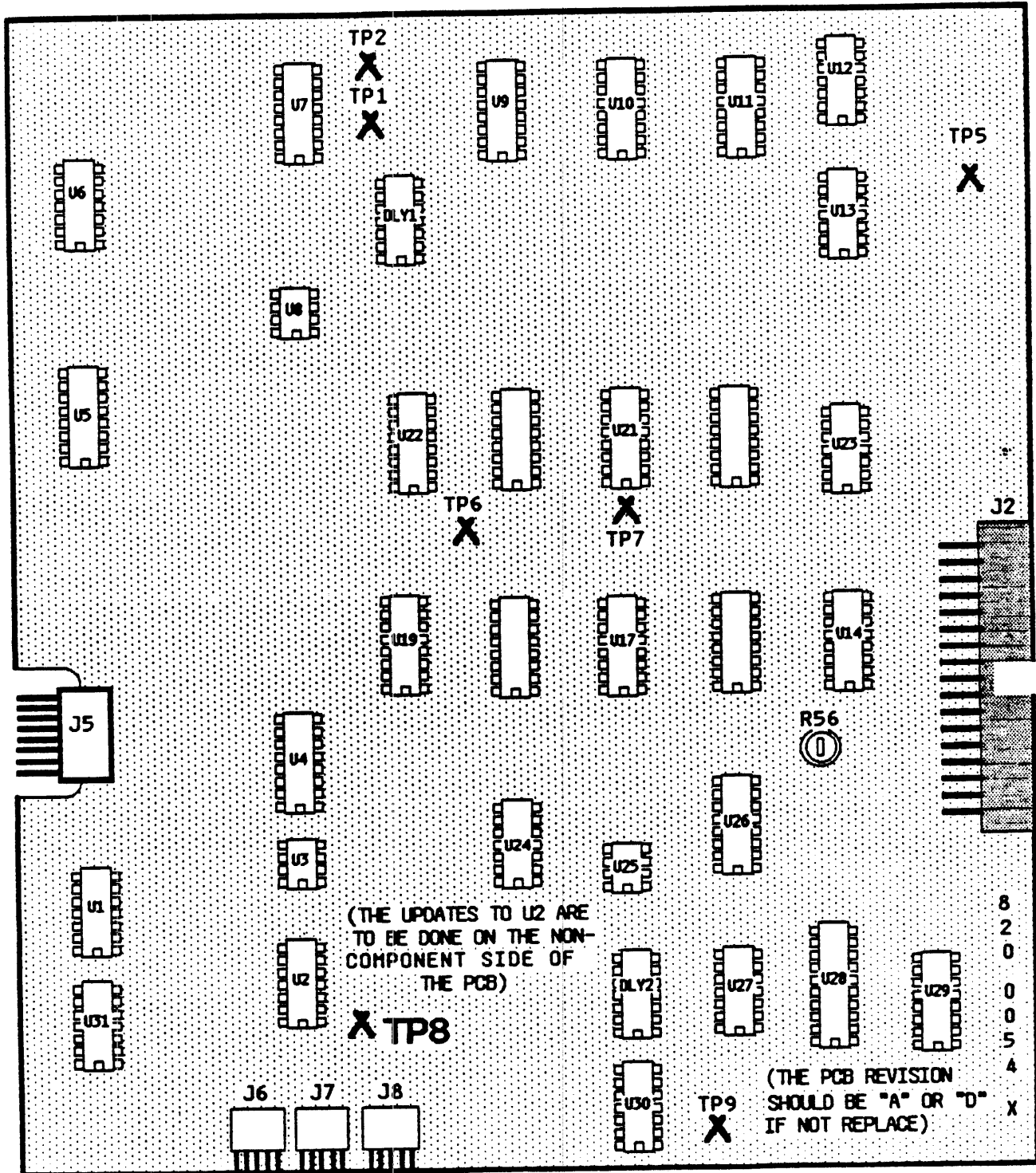
<u>PART</u>	<u>APPLE PART NUMBER</u>
5.1K ohm Resistor (1)	101-4512
0.1 microfarad Capacitors (2)	130-0007
1K ohm Resistor +5% (1)	101-4102
6.36 X 5/16 Standoff (1)	860-0213
Masked Z8 Microprocessor (1)	341-0171-A
330 ohm DIP Packs (2)	112-0105

Identify the Rev level etched on both sides of the PCB. Refer to the illustration on the opposite page for the location of the items mentioned in the following discussion. If the Rev is 820-0055 Rev A, B, C, or D then perform the following checks and upgrades.

(There are a few controller PCBs in the field that do not have the 820-0055 number etched on the PCB. These PCBs should be replaced with an 820-0055 rev PCB.)

- A. Solder a 5.1K ohm resistor (PN 101-4512) between pins 1 and 3 of connector P3 on the controller bd.
- B. Solder a 0.1 uf capacitor (PN 130-0007) between pins 3 and 5 of connector P3 on the controller.
- C. Solder a 0.1 uf capacitor (PN 130-0007) between the upper lead of R14 (U40 pin 2) and the bottom lead of C36 (ground).
- D. Check that R15 is present on the PCB. If R15 is missing or one lead is cut then replace it with a 1K ohm 5% resistor (PN 101-4102).
- E. Check that the metal standoff between the controller PCB and the power supply assembly is 5/16" in length. If it is not, replace it with a 6-36 X 5/16" standoff (PN 860-0213).
- F. Check that U1 and U2 on the controller PCB are between 330 and 332 ohm DIP packages. If they are any other value, then replace them with 330 ohm DIP packages. (You may wish to verify the resistance of the current DIP packages with an ohm meter.)
- G. Check the Z8. If it is the piggyback version then replace it with the latest mask version (no piggyback) (PN 341-0171-A).

# ANALOG PCB



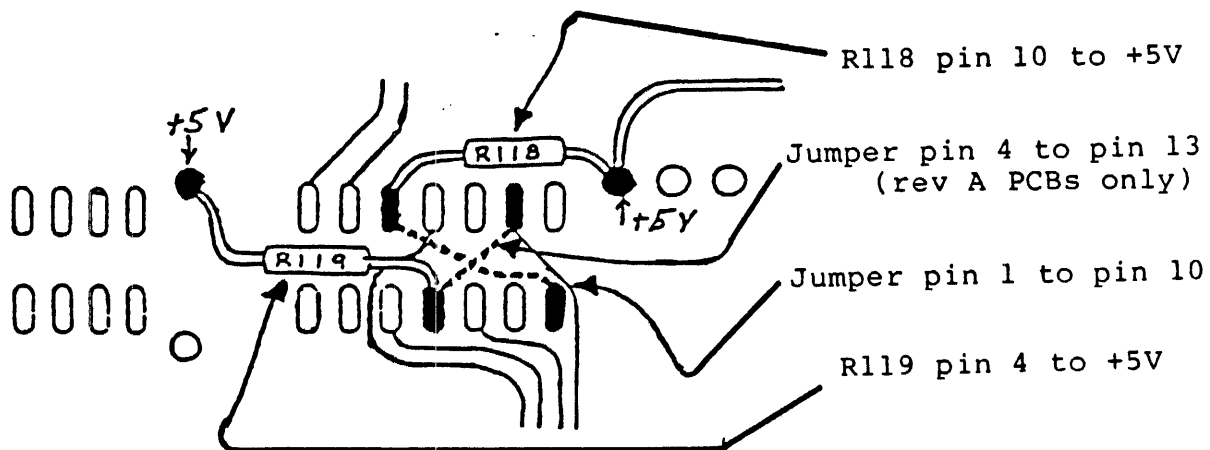
## ANALOG BOARD UPGRADE PROCEDURE

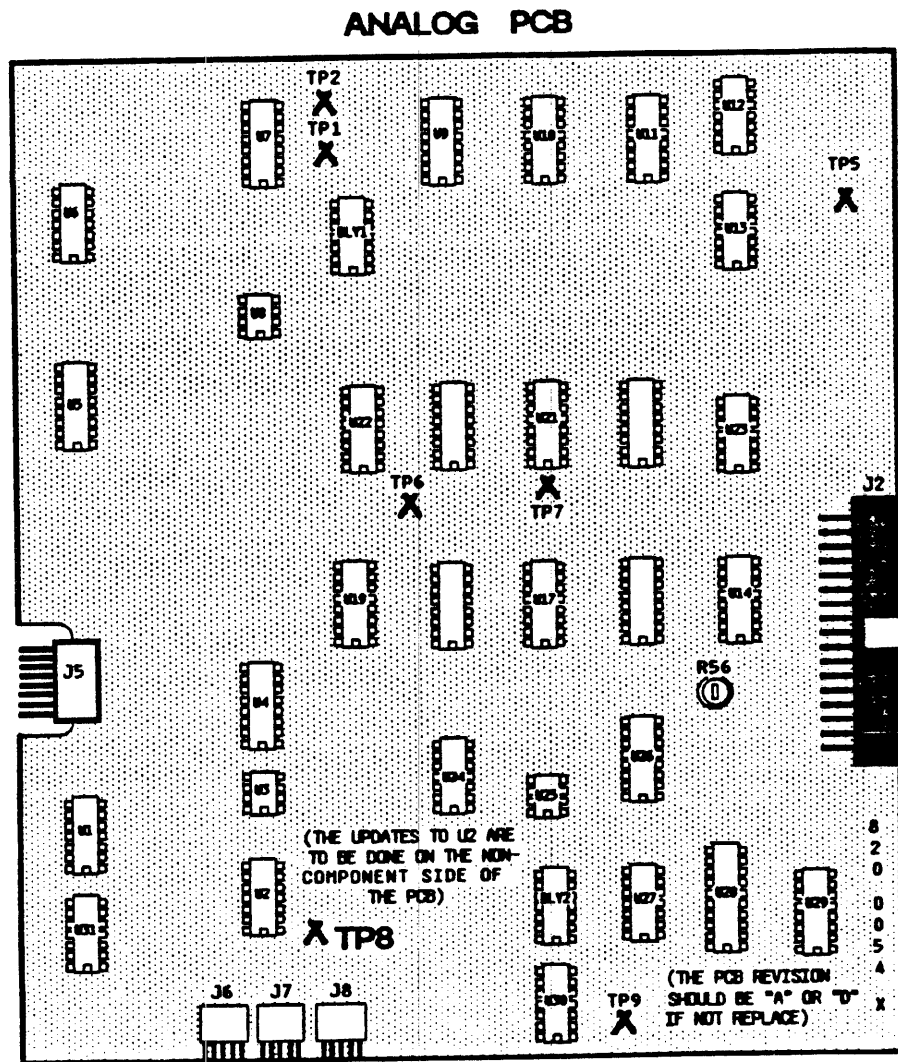
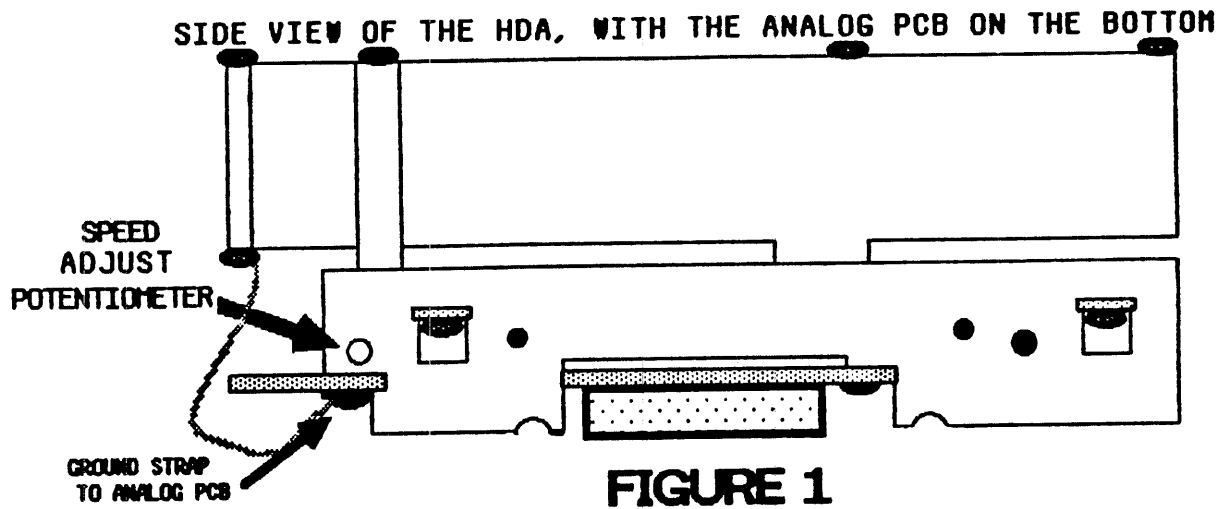
The following equipment may be needed to perform this procedure:

PART	APPLE P/N
20mm section of 26 to 30 gauge insulated wire	N/A
12mm section of 26 to 30 gauge insulated wire	N/A
3.9K ohm Resistors (2)	101-4392

1. Identify the rev level of the PCB. The PCB part number is etched at the bottom left on both sides of the PCB. The number will be either 820-0054-A (rev A) or 820-0054-D (rev D). (No rev "B" or rev "C" PCBs were ever made for production) There are a few older analog PCBs in the field that do not have the 820-0054 number and alphabetic (i.e A, or D) identifier etched on the PCB. These should be replaced with rev "A" or "D" PCBs.
2. Locate device U2 and turn the PCB over.
3. If the PCB is rev "D", this will be the final step (skip step 4). If the PCB is rev "A" perform both this step and step 4.
  - A. Solder an insulated wire approximately 3/4 (15mm) long from pin 1 of U2 to pin 10 of U2.
  - B. Solder a 3.9K ohm resistor (Apple PN 101-4392) between pin 10 of U2 and +5V. This will be designated R118 on updated schematics.
  - C. Solder a second 3.9K ohm resistor from pin 4 of U2 to +5V. This will be designated R119 on updated schematics.
4. Solder an insulated wire approximately 1/2" (9.5mm) long from pin 4 of U2 to pin 13 of U2.

### Underside of Analog PCB Location U2





**FIGURE 2**



## HDA SPEED CHECK AND ADJUSTMENT PROCEDURE

The following equipment will be needed to perform this procedure:

---

Frequency Counter and probes  
Anti-sabotage Sealant (e.g. glyptol)  
Tweaker (1) for adjusting potentiometers

---

Note: If you need instructions for any removal/replacement, you can find them in the Module Removal/Replacement Procedures part of this section.

### To CHECK:

- (1) Remove the cover from the Profile.
- (2) Connect the black lead from the frequency counter to a ground point on the analog PCB. Connect the red lead to TP-1 on the Controller PCB.
- (3) Set the frequency counter to read Per. A @ 10 hz.
- (4) Turn on the Profile and allow 30 seconds for the HDA motor to get up to speed. The frequency counter should be showing the motor speed to be within 1% of 16667 ms. (16500 to 16832 ms.) If the motor speed is not within this range then perform the adjustment procedure below. If the motor speed is within the proper range reinstall the HDA assembly and cover on the Profile.

### To ADJUST:

- (1) Remove the HDA assembly from the Profile. Once removed, reconnect the ribbon cable from the HDA to P2 on the Controller PCB, and power connector P4 from the Power Supply to the HDA.
- (2) Locate the trimmer potentiometer positioned near the ground strap on the Analog PCB by P4.
- (3) Adjust the trimmer potentiometer until the HDA motor speed is within range (after each turn of the potentiometer allow time for the motor speed to settle).
- (4) Once the motor is within the specified limits, lock the adjusting screw on the trimmer pot with anti-sabotage sealant.
- (5) Reinstall the HDA assembly and cover.

## INDEX CHECK AND ADJUSTMENT PROCEDURE

The following equipment will be needed to perform this procedure:

---

5/64 Allen (hex) driver  
.030 inch flat gauge

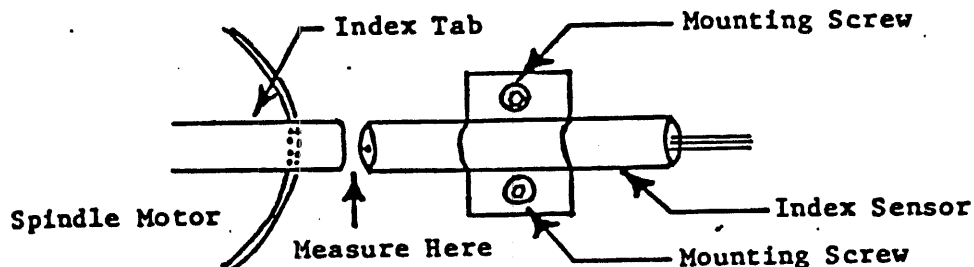
---

Note: If you need instructions for any removal/replacement, you can find them in the Module Removal/Replacement Procedures part of this section.

### To CHECK:

- (1) Remove the Cover, and then the HDA assembly, from the Profile.
- (2) Remove the Analog PCB from the HDA.
- (3) Turn the HDA upside down in front of you. Locate the index mechanism as shown in figure 1 below.
- (4) Rotate the spindle motor until the silver index tab on the spindle motor is aligned with the index sensor.
- (5) Slide the gauge into the gap between the silver index tab on the spindle motor and the index sensor. If the gap is too small for the gauge, or the gauge is not snugly held in the gap, perform the adjustment below. If the gap is OK, reinstall the Analog PCB on the HDA assembly and the HDA assembly in the Profile. Then reinstall the Cover.

### INDEX MECHANISM



(Fig. 1)

(This procedure is continued on the next page.)

INDEX CHECK AND ADJUSTMENT PROCEDURE (continued)

**To ADJUST:**

- (1) Loosen the two mounting screws so that the index sensor moves freely.
- (2) Align the silver index tab and the index sensor.
- (3) Place the 30 mil. flat gauge between the index tab and the index sensor.
- (4) Push the index sensor forward (towards spindle motor) until it makes light contact with flat gauge.
- (5) Tighten the mounting screws.
- (6) The flat gauge should be held firmly but should not be so snug that it cannot be easily removed.
- (7) Remove the flat gauge and check the operation of the index sensor.
- (8) Reinstall the Analog PCB into the HDA assembly, and the HDA assembly into the Profile.

## BRAKE CHECK AND ADJUSTMENT PROCEDURE

The following equipment will be needed to perform this procedure:

---

5/64 Allen (hex) driver  
.010 inch flat gauge  
Locktite thread sealer

---

There are 2 main revisions of motor control PCBs for the Profile HDA. The older rev uses a brake to slow the HDA disk motor after power is removed. It is for this rev of motor control PCB that this procedure was developed. The newer rev reverse biases the disk motor to slow the disk after power is removed. You can identify which PCB you have by referring to the illustration on page 2.16.

Note: If you need instructions for any removal/replacement, you can find them in the Module Removal/Replacement Procedures part of this section.

### To CHECK:

- (1) Remove the Cover and then the HDA assembly from the Profile.
- (2) Remove the Analog PCB from the HDA.
- (3) Turn the HDA upside down in front of you. Locate the brake mechanism as shown in figure 1. Insert the flat gauge between the Solenoid Body and the Plunger Plate as shown in figure 1.

The gauge should fit snugly but slide easily.

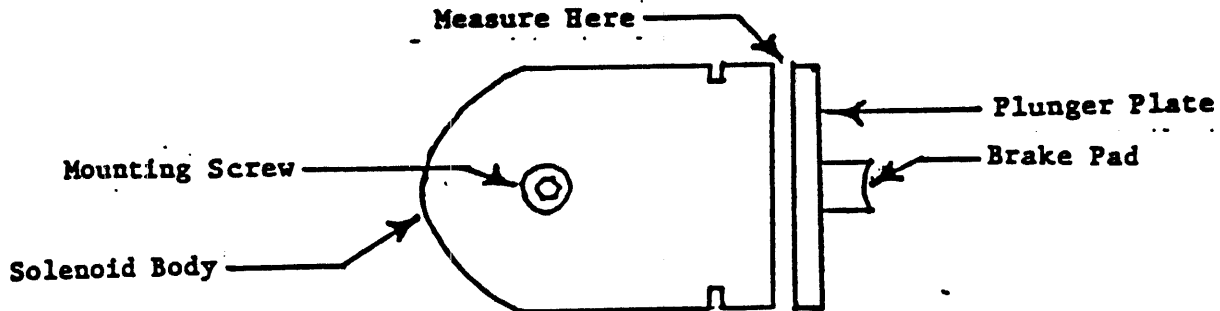
If the clearance is too tight or too loose, perform the procedure below.

If the clearance is OK reinstall the HDA assembly, and then reinstall the Cover.

(The adjustment procedure is continued on the next page.)

BRAKE CHECK AND ADJUSTMENT PROCEDURE (continued)

**BRAKE MECHANISM**



(Fig.1)

**To ADJUST:**

- (1) Remove the mounting screw and coat the end threads with locktite.
- (2) Carefully replace the mounting screw; avoid getting any locktite on the sides of the screw hole in the solenoid body.
- (3) Run in the mounting screw until snug, then back out 1/4 turn.
- (4) Place the flat gauge between solenoid body and plunger plate.
- (5) Push the solenoid body forward (toward spindle motor) until the brake pad makes light contact with the braking surface of spindle motor.

(Hint: an Allen driver or similar object placed through the screw hole in the side bracket behind the solenoid body provides a convenient method of positioning the solenoid).

(The adjustment procedure is continued on the next page.)

BRAKE CHECK AND ADJUSTMENT PROCEDURE (continued)

- (6) Tighten the mounting screw.
- (7) The flat gauge should be held firmly by the solenoid but should not be so snug that it can not be removed easily.
- (8) Remove flat gauge and check operation of the brake by performing the following steps:
  - a. Carefully position the HDA on a level surface, with the brake on top.
  - b. Reconnect P4 (no other HDA connections are necessary) from the HDA to the Power Supply.
  - c. Plug the Power cord into the Profile and turn it on.

**Observe:** That when the spindle motor begins to spin, the brake solenoid energizes and pulls the brake pad away from the braking surface of the spindle motor.

- d. Turn the Profile off.

**Observe:** That the brake solenoid deenergizes and the brake pad is released to contact the braking surface of the spindle motor.

**WARNING:** Disconnect Power from the Profile before going any further.

- (9) If the brake "chatters", a possible remedy is canting or tilting the solenoid body left or right.
- (10) Reinstall the Analog PCB on the HDA assembly, and the HDA assembly in the Profile.

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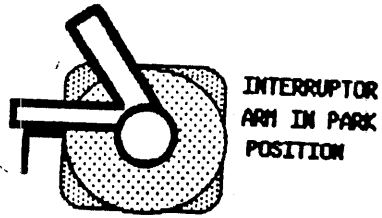


FIGURE 1

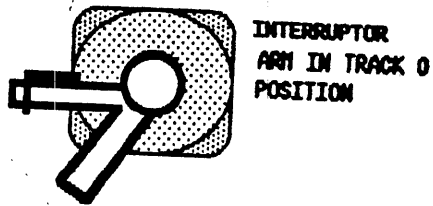


FIGURE 2

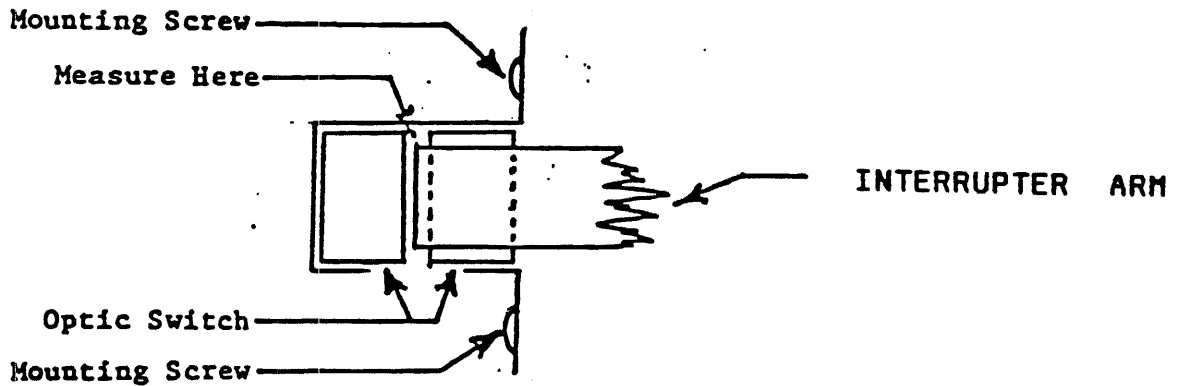


FIGURE 3



## TRACK 0 CHECK AND ADJUSTMENT PROCEDURE

The following equipment will be needed to perform this procedure:

---

Profile Debug Z8  
.010 inch wire gauge  
.070 inch wire gauge  
A/// with internal disk drive  
.050 inch Allen (hex) driver

---

Note: If you need instructions for any removal/replacement you can find them in the Module Removal Replacement Procedures in this section.

### To CHECK:

- (1) Remove the cover from the Profile.
- (2) Position the Profile so that the interruptor arm on the HDA is in front of you.
- (3) On the Controller PCB remove the system Z8 with masked ROM, and install a piggyback Debug Z-8 into its socket.
- (4) Turn on the Profile

**Observe:** That after approximately 20 seconds the HDA interrupter arm will move from Park position to track 0 position as shown in figures 1 and 2.

- (5) Use the .010 inch and the .070 inch wire gauges to insure that the clearance between the top of interrupter arm and optic mounting bracket (See Fig. 3) is between .010 and .070 inches. If it is not then perform the adjustment procedure on the next page.

NOTE: If the following adjustment does not work, try adjusting the position of the interrupter arm on its shaft to obtain the proper clearance.

(The adjustment procedure is located on the next page.)

TRACK 0 CHECK AND ADJUSTMENT PROCEDURE (continued)

To ADJUST:

- (1) Loosen the mounting screws on the optic bracket.
- (2) Slide the bracket/optic assembly towards the top of HDA to open the gap between the interrupter arm and the optic mounting bracket.
- (3) Slide the 50 mil. wire gauge into the gap, being careful not to disturb interrupter arm.
- (4) Slide the bracket assembly down until the top of the bracket and the interrupter arm close lightly on the gauge.
- (5) Carefully tighten mounting screws so as not to disturb the adjustment.
- (6) Turn off the Profile and replace the Debugger Z8 with the System Z8.
- (7) Turn on the Profile and wait approximately 2 minutes as it performs its Scan sequence. At the end of the Scan sequence the interrupter arm should be returned to the Park position.
- (8) Turn off the Profile.
- (9) On the Controller PCB remove the System Z-8, and install the piggyback Debug Z-8 in its socket.
- (10) Turn on the Profile and recheck the clearance between the optic bracket and the interrupter arm as described above. Reperform the adjustment until the clearance is OK.
- (11) Turn off the Profile and replace the Debug Z8 with the System Z8.
- (12) Reinstall the Cover on the Profile.

## HDA FORMATTING PROCEDURE

The following equipment will be needed for this procedure

---

Apple ///  
Profile Interface PCB for the Apple ///  
Profile Interface Cable  
Jumper (a 2 inch length of 22 ga. wire with small alligator clips at both ends will do)  
Debugger Z8  
Format software (Profile format diskette #889-0013)

---

1. Install the Profile Interface PCB in slot 1 of the Apple /// and connect the Profile Interface Cable from it to the Profile.
2. Remove the cover from the Profile. If instructions are needed refer to the Module Removal and Replacement Procedures in this section.
3. Remove the system program Z8 from the Controller PCB and insert a Debugger Z8. If at all possible do not remove the prom from the piggyback socket as this can cause intermittent failures because of damage to the piggyback socket.
4. Turn on the Profile and wait 30 seconds for the HDA motor to come up to speed.

**Note:** When the Profile is turned on, its firmware will flash the Ready LED as the power comes up. After that function is performed the firmware program in the Debugger Z8 will not turn the Ready LED on again until the program in the Apple /// initiates communications with the Profile.

*(If LED comes on steady at power on "and stays on", this symptom may indicate a bad E-PROM).*

5. Boot the Format program.

**Observe:** the Ready LED comes on steadily. If it does not, check all connections between the Apple /// and the Profile.

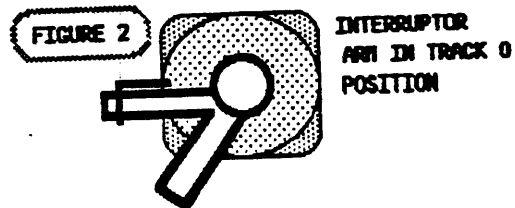
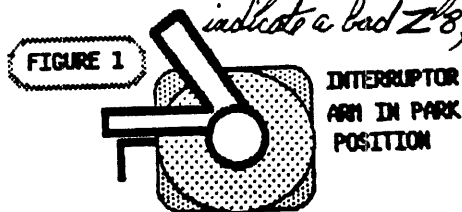
**Note:** the program may prompt you that the Profile has incorrect FD.ROM version 03.11. This is normal the Format program will work OK.

6. Press <RETURN>, then as prompted by the display, install the jumper to short the two pins of P7 on the Controller PCB together (refer to the illustration of the Controller PCB on page 2.18 to help you find P7).

**Note:** the statement "press any key", as now displayed, is incorrect, it should read "press RETURN" **THIS IS TRUE FOR THE REST OF THE FORMAT PROCEDURE**

7. Press <RETURN> and watch the interrupter arm on the Hard Disk Assembly (HDA), it should step from track 0 to the park position as shown below in approximately 180 seconds.

*NOTE: If after pressing RETURN the interrupter arm does not move and the screen immediately displays the message stated in Paragraph 8, below (as if it had successfully formatted), this symptom may indicate a bad Z'8, P/N 338-8603.*



**Note:** If the arm did not complete the scan swap the HDA to a known good Profile and retry. If Format still does not occur the HDA is probably faulty replace it.

8. After completion of the scan the screen display will tell you if the formatting was succesful or not. (if there was an error in formatting the screen will display an error code, recheck all connections on the Pro-File and between the Pro-File and the host computer.)

**Observe:** If the formatting was successful the Ready LED will come on steadily and the screen will display.

"Formatting completed. Pass  
Remove jumper. Press any key to continue"

**Caution:** At this time remove the jumper from P7 to prevent damage to the unit.

9. Press <RETURN> as prompted . The following should occur within the next 2 and 1/2 minutes:

**Observe:** The profile will now automatically:

- \* Scan all sectors, heads and tracks
- \* Compare buffers on track 77
- \* Certify all sectors on track 77
- \* Initialize spare tables on track 77

At the end of each process listed above the screen display should indicate "pass".

**Note:** the last line on the screen display "press <RETURN> when profile is ready" only indicates that if you have more than one profile to format, the diskette does not have to be rebooted each time.

### FINAL SYSTEM TEST (FST) PROCEDURE

The following equipment will be needed for this procedure

Apple ///	A/// Profile Interface PCB
FST Software (APN # 889-0029)	Profile Interface Cable

1. Install the Profile Interface PCB in slot 1 of the Apple /// and connect the Profile Interface Cable from it to the Profile.
2. Ensure that there is a system ROM Z8 installed on the Controller PCB.
3. Turn on the Profile and wait 2 minutes for the Pro-File to complete its Scan sequence.
4. Boot the FST program. Observe that for 10 minutes the Profile will write and verify each track in sequence from track 0 to track 152 (the Ready LED will blink as each operation occurs). You should see a screen like the one below.
5. Run FST for the specified period (15 minutes, or 48 hours). If an error line occurs (described below) determine if it is fatal by checking the MAX ERRORS ALLOWED column for the error code on the Criteria Sheet on the opposite page.
6. To terminate the test press <ESCAPE>.

P	FINAL SYSTEM TEST														
	TOTAL BLOCKS	TOTAL	I/O				PIPPIN				COM	LOGICAL	PHYSICAL		
	TRANSFERRED	ERRORS	STATUS				STATUS				TIME	BLOCK	CYL	HEAD	SECTOR
			R1	R2	R3	R4	S1	S2	S3	S4			g	g	g
→ R	aaaaaaa	bbbbbb	cc	cc	cc	cc	dd	dd	dd	dd	eeee	ffff	gg	g	gg

The STATUS LINE reflects the conditions occurring during the current block transfer. The values in the STATUS LINE should always be changing as FST exercises the Profile.

a = Total number of blocks transferred during the test. This number will be continuously incrementing as long as the test is being run.
b = Total errors that have occurred throughout the test. This number should equal the number of error lines at the bottom of the FST screen.
c = These bytes relate to the I/O status bytes the Profile sends to the host operating system during communications.
d = These bytes relate to the particular status code/s that were sent from the Profile to the host (FST test program).
e = Indicates the time elapsed for the current block transfer.
f = The Logical block sent by the host (FST test program).
g = Indicates the Cylinder (Track), Head, and Sector being read from or written to.

IF AN ERROR OCCURS, THE STATUS LINE FOR THAT ERROR WILL BE PERMANENTLY DISPLAYED AT THE BOTTOM OF THE FST SCREEN. THE ERROR CODE IS TAKEN FROM THE "d" FIELD AS DESCRIBED ABOVE. YOU MAY INTERPRET THIS ERROR BY COMPARING IT TO THE CRITERIA SHEET ON THE OPPOSITE PAGE. A MORE DETAILED EXPLANATION MAY BE FOUND ON PAGE 2.58 AND 2.59. THE LOCATION OF THE SECTOR THE ERROR OCCURRED ON MAY BE FOUND IN THE "g" FIELD OF THE ERROR LINE.

→ R	aaaaaaa	bbbbbb	cc	cc	cc	cc	dd	dd	dd	dd	eeee	ffff	gg	g	gg
-----	---------	--------	----	----	----	----	----	----	----	----	------	------	----	---	----

# FINAL SYSTEM TEST (FST) CRITERIA SHEET

10/20/83

FINAL SYSTEM TEST (FST) ERROR STATUS CODES	MAX ERRORS ALLOWED
00 02 00 00 ↑ SEEK TO WRONG TRACK	6
00 00 00 00 ↑ CAN'T READ 3 SECTORS AFTER SEEK	0
00 02 00 00 ↑ SEEK TO WRONG TRACK ↑ CAN'T READ 3 SECTORS AFTER SEEK	0
04 00 00 00 ↑ CAN'T FIND TARGET HEADER IN 9 REVS	0
04 04 00 00 ↑ SPINDING OCCURRED ↑ CAN'T FIND TARGET HEADER IN 9 REVS	2
04 08 00 00 ↑ UNABLE TO READ STATUS SECTORS ↑ CAN'T FIND TARGET HEADER IN 9 REVS	0
05 00 00 00 ↑ CAN'T FIND TARGET HEADER IN 9 REVS REQUESTED OPERATION FAILED	0
05 00 00 00 ↑ CAN'T READ 3 SECTORS AFTER SEEK ↑ CAN'T FIND TARGET HEADER IN 9 REVS	0
08 00 00 00 (<1 TO 09> (SEE NOTE 3)) ↑ SOFT READ ERROR	99
08 00 00 (<10 OR HIGHER> (SEE NOTE 3)) ↑ HARD READ ERROR	8
08 04 00 00 ↑ SPINDING ROUTINE ↑ READ ERROR	10
09 00 00 00 ↑ READ ERROR OR REQUESTED OPERATION FAILED	10
10 00 00 00 ↑ CAN'T READ 3 SECTORS AFTER SEEK ↑ CAN'T READ 3 SECTORS AFTER 2 RESEKES	0
15 00 00 00 ↑ CAN'T READ 3 SECTORS AFTER SEEK ↑ CAN'T FIND TARGET IN 9 REVS OR REQUESTED OPERATION FAILED ↑ CAN'T READ 3 SECTORS AFTER 2 RESEKES	0
15 02 00 00 ↑ SEEK TO WRONG TRACK ↑ CAN'T READ 3 SECTORS AFTER SEEK ↑ CAN'T FIND TARGET IN 9 REVS OR REQUESTED OPERATION FAILED ↑ CAN'T READ 3 SECTORS AFTER 2 RESEKES	0
60 00 00 00 ↑ 3 BYTE SEPARATOR BETWEEN WRITE BUFFER AND STATUS TABLES OR S2-3 SET. SPINNE TABLE UPDATE OCCURRED. BUFFER DATA IS CHANGED.	0

**NOTES:**

1. A "BLOCK ID MISMATCH" OR A "BUFFER COMPARE FAILED" IS NOT ALLOWED
2. ANY COMBINATION OF ERRORS EXCEEDING 99 TOTAL IS NOT ALLOWED
3. BRACKETS INDICATE A RANGE OF NUMBERS THAT CAN OCCUR

## QUICK DEBUGGER TEST PROCEDURE

The following equipment will be needed for this procedure

---

Apple ///  
Profile Interface PCB for the Apple ///  
Profile Interface Cable  
Quick Debugger Software Version E00.07 (APN# 889-0004)  
Silentype Printer

---

The Quick Debugger program reads the spares table from the Pro-File and prints the original sector location of every spared sector listed in that table.

1. Install the Profile Interface PCB in slot 1 of the Apple /// and connect the Profile Interface Cable from it to the Profile.
2. Ensure that there is a Z8 with standard system ROM installed on the Controller PCB.
3. Turn on the Profile and wait 2 minutes for the Pro-File to complete its Scan sequence.
4. Connect the Silentype to Port A on the back of the Apple ///.
5. Boot the Quick Debugger program.

**Observe:** The Quick Debugger command prompt line is displayed as shown below.

```
COMMAND (B,F,P,Q,R,S,T,V,W,?)=>
```

6. Type <S> to select the Get Status command.

**Observe:** a. The line shown below is displayed next to the command prompt line.

```
00          STATUS-GET STATUS BLOCK 00 00 00 00 00 00 00
```

b. The Ready LED goes out as the interrupter arm on the HDA goes to track 77 to read the spares table.

c. A new command prompt line is displayed.

(continued on the next page)



7. Type <P> to select the Print Status command.

Observe: The line shown below is displayed on the CRT.

PRINT STATUS TO SCREEN OR PRINTER (S/P)

8. Type <P> to select the printer.

Observe: The Silentye prints out as shown below.

CONTROLLER VERSION - 03.98

SPARED SECTOR  
TOTAL 00

LIST CYL HD SECT

BAD BLOCKS  
TOTAL 00

LIST CYL HD SECT

(End of this procedure.)

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## PART 1 INTRODUCTION

The Formatter/Debugger program is provided as a service aid for troubleshooting block I/O devices such as the ProFile disk drive. It is a program that allows you to directly communicate with a block I/O device and exercise it through a series of unique commands or build simple test sequences that will assist in debugging the device.

It is a particularly helpful tool for servicing devices that have been returned because of a malfunction, etc.

For example, the program can be used to detect an error and then by using the loop on error function, you can use an oscilloscope to analyse the circuit that caused the error.

You can use the program to service a drive containing either the Format/Debugger ROM Z8 or the Standard System ROM Z8. (The Standard System ROM Z8 is the operational ROM in the Z8 that is shipped in the disk drive.) The command summary, part 3, specifies which type of ROM must be in the drive to use a given command.

### PART 1.1 HOW TO USE THIS PROGRAM

To use this debugger properly, you should be aware of some of the design concepts. In designing the user interface (command structure) it was decided to use single character commands (explained later). This permits you to type in the command very rapidly and use options (which are not always required) to modify certain test variables.

The most used test variables are the three byte logical block that is treated as either a 24-bit number or as three 8-bit numbers. As a 24-bit number, the variable represents a standard logical block with a decimal range of 0-16 million blocks (Hex 000000- FFFFFFFF). As three 8-bit numbers, each variable has a range of 0-255 (Hex 00-FF).

The program makes no assumptions about the use of the test variable; it just gives you two ways to talk to it.

You can consider it as a large (24 bit) number or as three smaller (8 bit) numbers. This variable is sent to the disk exactly as a 24-bit number which the firmware decides how to interpret.

You, the user, must know how the firmware will react to understand what the firmware is doing with the block number.

## PART 1.2 TYPICAL COMMAND EXAMPLES

**NOTE:** Data shown in <> is meant to be typed.  
Data shown in [] or () is optional.

To help make the concept of this program more clear, here are some examples that show what the more common commands do.

<R>           (Read)

This command requests data to be read from the unit being tested. It passes the command and the BLOCK variable to the unit and transfers the data from the unit to the input buffer (see the display command, part 2.2.3, for information on displaying the input buffer).

R by itself does not change the BLOCK variable; it uses its current value. However, you can change the block variable by adding a modifier to the command in the form of a number.

This number is normally treated such that leading zeros are assumed, thus 0, 00, 0000, etc. all produce the 24-bit value 000000. For example:

R0 or R00 or R000000, etc.           (read block 000000)  
R13 or R013 or R 0013, etc.       (read block 000013)

The above example is applicable only when using the Standard System ROM Z8. Notice that the BLOCK variable sent is either 000000 or 000013.

The number 13 is the same as 013 or 000013 and produces the value 000013 in the BLOCK variable.

**NOTE:** The number 13 in the example is a HEX number, not a decimal number.

13 Hex = 19 Decimal

Remember that the firmware in the disk drive being tested determines how the BLOCK variable will be treated. Normally it is treated as a logical block.

In the example on the following page, let's change the command to show how it would be used with the Format/Debugger ROM Z8:

For example: <RT1H2S3> or <RT01H02S03>, etc. (read block 010203)

Notice that the command now has 3 modifiers in the form of T and a number, H and a number, and S and a number.

The modifier T (Track) references the first 8-bits of the BLOCK variable, the H (Head) references the second 8-bits, and the S (Sector) references the third 8-bits.

Note that they are separate modifiers and can be used independently.

For example:

If BLOCK = 000000, then the command <RT5><RETURN>  
will set BLOCK = 050000

If BLOCK = 050000, then the command <RH3><RETURN>  
will set BLOCK = 050300

If BLOCK = 050300, then the command <RT16S9><RETURN>  
will set BLOCK = 160309

Note that the last command in the example happened to affect the first and third bytes. Had the last command been RS9 then the BLOCK would have been 050309.

When all three modifiers are used, they must be in the T, H, S sequence.

REMEMBER! The numbers used are always Hexidecimal numbers.

<W> (write)

This command requests data to to be written to the unit being tested.

It passes the command and the BLOCK variable to the unit and transfers the data to the unit from the output buffer (see the buffer fill command, part 2.2.1, and the display command, part 2.2.3).

W by itself does not change the BLOCK variable; it uses its current value. However, as was the case with a read command, the BLOCK variable can be changed by adding a modifier.

For example, the commands W0, WT3H2S1, WH9, etc. have the same effect on the BLOCK variable that they do in the Read command.

<+> (plus)

This command increments the BLOCK variable. + by itself increments the variable by 1. For example, if the BLOCK variable was 00001F, then after + it will be 000020 (Note the hex numbers). +3 will increment the BLOCK by 3 each time. +3T will increment the first 8-bit variable by 3 each time. For example, if the BLOCK was 050311, then +3T will change it to 080311. H and S work the same way to modify the second and third groups of 8-bit variables.

To provide wraparound and carry, the + command will wrap a 24-bit number at FFFFFF. It will wrap T at 97 (97 increments to 0) and will set H and S to 0 to provide full wrap. H will wrap at 3 (3 goes to 0) creating a carry to T and S will wrap at F (F goes to 0) creating a carry to H. Future enhancements will be to find out what the maximum block count for a device is and then wrap the 24-bit number at that count.

<D> (Display)

This command displays the contents of the input or output buffers.

- D by itself will display the input buffer.
- DI is the same as D.
- DO will display the output buffer.
- DS will decode the contents of the input buffer as extended status information.

The form of the display is the same as that for an APPLE monitor memory dump. It will display the first 256 bytes of the buffer and pause so that you can study the values.

At the bottom of the screen it asks for <ESCAPE> to terminate, <RETURN> to quit, ANY other key to continue.

<ESCAPE> stops further display and cancels the rest of the command line effectively stopping processing and returning control to the user.

<RETURN> quits the display command and causes the program to go on to the next command.

Pressing any of the other keys, except the space bar, will allow the program to display the next 256 bytes of the buffer.

Pressing the space bar will allow you to display the buffer line by line.

**CAUTION:** If you just keep hitting a key to see the next 256 bytes you will see first the buffer you requested and then memory above it. There are areas of ram above the buffers that will, when displayed cause your screen to get VERY sick and you will have to either re-boot the program or be very familiar with APPLE III hardware and monitor.

Just in case you are not familiar with the monitor memory display, here is an example. (The monitor doesn't display the descriptive information above the dashed line.)

Hex																
Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8000:	00	1A	23	92	FF	FE	A5	2F	33	34	00	00	00	00	00	00
8010:	12	11	34	87	FE	44	00	00	3E	4C	00	20	A9	0F	C5	00
etc.																

## PART 2. COMMAND STRUCTURE

Each command consists of one or more characters and modifiers in command groups.

Each group is separated by one or more spaces.

The command line is one or more command groups.

There is enough space in the command buffer for 255 characters.

Multiple command lines are possible by use of the Macro Add command.

### PART 2.1 COMMAND PROMPT

The program prompt consists of the following two lines:

```
S1 D1  
COMMAND (B,C,D,F,G,H,I,L,M,N,O,P,Q,R,S,T,V,W,X,+,-,/, ?) =>
```

The first line contains two flags, S1 D1, that tell which slot and drive the program is set to test.

The second line of the prompt consists of the first letter of each valid command. A list of the commands is always available by typing H or ? and pressing <RETURN>.

NOTE: After typing a command and pressing <RETURN> to execute it, you can press <ESCAPE> to terminate the command.

However, if you wish to review the command that you just executed for the purpose of changing it, etc., you can simultaneously type <CONTROL> <A> instead of <ESCAPE>.



## PART 2.2 DETAILED COMMAND DESCRIPTIONS

Following are descriptions of some of the commands that require more detailed explanations than others. In depth examples of some of the more commonly used commands such as Read, Write, Increment, and Display were provided in part 1.2. For an overall summary of all commands, refer to part 3.

### PART 2.2.1 BUFFER FILL

<B>[num]<RETURN>

- where num is an optional 16 bit hex number  
(eg.,B0123)

The buffer fill command is used to fill the output buffer with a specific data pattern. It can be used with either the Format/Debugger ROM Z8 or the Standard System ROM Z8 installed in the drive. To use the command, type B followed by a number which will be treated as a 16 bit (2 byte) pattern.

For example, the command

<R0><sp><B1234><sp><W0><sp><B45<sp><W1><RETURN>

would read logical block-0, fill the output buffer with 12341234..., write block-0, fill the output buffer with 00450045..., and finally write this data to block-1.

### PART 2.2.2 CREATE SPARE

<C><RETURN> ---- the C-command must be the only command on the line.

The create spare command is used to force a peripheral device to transfer a logical block to a new (spare) physical location on the device. The command will then request the block number to be spared and will then request confirmation from the user. If confirmed, the logical block will be spared by the device controller. This command should only be used when the Standard System ROM Z8 is installed in the drive.

Using this command will allow you to fix flaky blocks found during testing. The user will be asked for confirmation of this command. Respond with Y (Yes) or N (no).

NOTE: Do not attempt to use the create spare command when the Format/Debugger ROM Z8, version D3.11 or earlier, is installed in your drive.

### PART 2.2.3 DISPLAY

<D>[I,O,S]<RETURN> - where I is input buffer, O is output buffer, and S is the extended status information in the input buffer.

The display command can be used with either the Format/Debugger ROM Z8 or the Standard System ROM Z8 installed in the drive. It is used to display the contents of the input or output buffers.

These buffers occupy the following Hex locations in the computer's memory:

input buffer ----8000H - 8213H  
output buffer ---8300H - 8523H

The display will show 256 bytes at a time, scrolling to the next 'page' after each key press.

To end the display and continue executing the command line, press <RETURN>.

To abort the command line press <ESCAPE>.

With the display on the screen, you can press the spacebar to cause a scroll to the first line of the next 'page'. Then, each time you press the space bar, the display will scroll one line forward.

The Display Status command works only slightly differently in that it decodes the input buffer into Extended status info about the spares and bad blocks and it will not stop until it is finished or until the space bar, <RETURN> key, or the <ESCAPE> key are pressed.

REMEMBER! The Display Status command will decode anything found in the input buffer so be sure to use the Get Status command first to make sure that the information is valid.

Before using the Display Status command with the Format/Debugger ROM Z8 installed, you must initialize the spare tables (see part 2.2.6) and then use the Get Status command, otherwise the display will contain garbage.

With the Standard System ROM Z8 installed, you only have to issue the Get Status command before displaying the extended status of the input buffer.

Here are some additional tips about using the Display Status command.

- After typing D[S] and pressing <RETURN>, press the space bar to stop the listing. Press the space bar again each time you wish to step through another line of the listing. Pressing any other key will cause a fast scan of the listing.
- Pressing <ESCAPE> will cancel the rest of the display function.
- Pressing <RETURN> will terminate the spare sector listing and start the bad block listing.

#### PART 2.2.4 FORMAT

<F><RETURN> ---- this command must be the only command in the command line.

The Format command is used with the Format/Debugger ROM Z8 installed in the drive. It is used to erase all old data from memory and lay down a new pattern of address and data.

After formatting a drive with the Format/Debugger ROM Z8 installed, you can type D[I] to get a list of the defective blocks. The list will end with FF FF FF FF. Refer to the documentation provided for the F/D ROM for further details. **WARNING:** This command is very dangerous and should only be used if damage to the address headers has occurred and only after every reasonable attempt has been made to recover other data from the device. The user will be asked to confirm this command. Respond with <Y> (Yes) or <N> (No).

Remember! This command will erase all previously recorded data.

Following is an example of the error message that will be displayed if you attempt to format a drive with a Standard System ROM Z8 installed.

---

					I/O			ProFile							
	Block				R1	R2	R3	R4	S1	S2	S3	S4	S5	S6	
FORMAT	S1	D1	00	03	5F	00	00	00	00	55	55	55	55	00	00

---

The 55's in this example are the error indicators.

### PART 2.2.5 GET STATUS

<G><RETURN>

The Get Status command works only with the Standard System ROM Z8. It is used to obtain extended status information from the drive and place it in the input buffer.

(You will need to execute the Display command to view the contents.)

The Get Status command makes sure that the status you are going to view is valid.

When using a ProFile you can also get the status by reading block FFFFFFFF.

### PART 2.2.6 INITIALIZE SPARE TABLE

<I><RETURN> ---- this command must be the first command in the command line.

The Initialize command is used by the ProFile Format/Debugger ROM Z8 to setup the spare tables in the ProFile drive.

After the Debugger ROM has formatted the disk, the entire disk is available to read from or write on so that certification of the entire disk is possible.

After the spare table sectors have been certified, the tables need to be initialized to allow the controller ROM to work properly.

The Initialize command is not used when the Standard System ROM Z8 is installed in the drive.

**WARNING:** This command is potentially dangerous as it effectively erases any old spared table data and if used incorrectly will cause the loss of valuable data on the ProFile.

The user will be asked to confirm this command. In response, type <Y> (Yes) or <N> (No).

### PART 3 COMMAND SUMMARY

Following is a summary of all the commands that can be used with this program:

**BUFFER FILL**      B[<RETURN>] or B[num]<RETURN>

Fill the output buffer.  
where num is a 16 bit hex fill number  
used with both Formatter/Debugger and Standard  
System ROM Z8s

**CREATE SPARE**      C<RETURN>

Force the drive to spare the specified block.  
must be the only command on the command line  
used only with Standard System ROM Z8

**DISPLAY**      <D><RETURN> or <D>[I]<RETURN> or  
                 <D>[O]<RETURN> or<D>[S]<RETURN>

Display the I/O buffers.  
used with both Formatter/Debugger  
and Standard System ROM Z8s

**FORMAT**      <F><RETURN>

Format the device.  
This is a dangerous command  
used only with Format/Debugger ROM Z8

**GET STATUS**      <G><RETURN>

Get extended status information.  
Remember! When using the ProFile, RFFFFFF (read  
block FFFFFFF) also returns status  
information  
used only with the Standard System ROM Z8

**HELP** <H><RETURN> or <H>[E]<RETURN> or  
<H>[E2]<RETURN> or <H>[char]<RETURN>

Print a list of commands, or errors, or a detailed description of each command.

Where **E** is to display errors when the Standard System ROM 28 is installed.

Where **E2** is to display errors when the Format/Debugger ROM 28 is installed.

Where **char** is any legal command shown in this command summary.

**INITIALIZE SPARE TABLE** <I><RETURN>

Clear the spare block table.

this is a dangerous command  
must be the first command on the command line  
used only with Format/Debugger ROM 28  
requires confirmation (Y or N)

**LOOPON** <LPF>[S,H,D]<RETURN>

Send Loop on Format commands to the firmware.

where **S** = sector marks  
**H** = address headers  
**D** = data field

LPF can be followed by any combination of  
**S**, **H**, and **D**  
executed following a Read Track command to  
loop on format of the current track  
(eg., R[T] reads the T byte of the block  
variable to determine the current track)  
used only with Format/Debugger ROM 28

**MACRO** <M>[A(0-9),C,L,0-9]<RETURN>

Use macro functions (alternate command lines).

where **A** = add current line to macro table  
**C** = clear all macros  
**L** = list macros

used with either Formatter/Debugger or  
Standard System ROM 28  
not effectively implemented at this time

N,O Not implemented yet

PAUSE <P>[<RETURN>] or  
<P>[A(num),C,(num),E(num),N(num)]<RETURN>

Pause and wait for user.

Where A = any error/nonerror  
C = clear any error/nonerror  
E = on error  
N = on no error  
(num) is a 16-bit mask of S1 S2

Note: All four digits of the 16-bit mask must be turned on

used with either Formatter/Debugger  
or Standard System ROM Z8

QUIT <Q>[<RETURN>]

Return to calling routine (This module is a subroutine).

READ <R>[(num),T(num),H(num),S(num)]<RETURN>

Read a block

where (num) = 24 bit number (8 bit if T,H,S)  
T = first (Hi) byte of block  
H = second (Mid) byte of block  
S = third (Lo) byte of block

Remember! The firmware of the device tested determines how the number is treated. See the following example:

T H S - Formatter/ Debugger ROM  
ProFile 00 00 00  
Hi Mid Lo - Standard System ROM Z8  
>0 means read to the output buffer ( Eg., R23>0 )  
used with either Formatter/Debugger or  
Standard System ROM Z8

**SCAN**      <S><RETURN>

Order the firmware to scan the entire disk (read only).  
Requires confirmation (Y or N)  
after scanning, use D[I] to get list of any bad blocks  
found during scan  
used only with Format/Debugger ROM Z8

**TURN OFF STEPPER**      <T><RETURN>

Turn off the power to the stepper motor.  
used with Format/Debugger ROM Z8 but not normally used  
with Standard System ROM Z8

**V**      Not implemented yet

**WRITE**      <W>[(num),T(num),H(num),S(num)]<RETURN>

Write to a block (same format as read).  
where (num) = 24 bit number (8 bit if T,H,S)  
T = first (Hi) byte of block  
H = second (Mid) byte of block  
S = third (Lo) byte of block

Remember! The firmware of the device tested determines  
how the number is treated. See the following  
example:

T    H    S    - Formatter/ Debugger ROM  
Profile    00    00    00  
Hi Mid    Lo    - Standard System ROM Z8

<I means write from the input buffer ( eg., W23<I )  
used with either Formatter/Debugger or  
Standard System ROM Z8



**XECUTE** <X><RETURN> or X[E(num)]<RETURN>

Execute the current command line again.

where E = execute the line to this point on error

num = 16 bit error mask of S1 S2

X[E] will execute a function over and over again,  
if an error has occurred, up to the point where  
the error occurred

**+** <+>[(num),T(num),H(num),S(num)]<RETURN>

Increment the block number.

where (num) = 24 bit number (8 bit if T,H,S)

T = first (Hi) byte of block

H = second (Mid) byte of block

S = third (Lo) byte of block

**-** <->[(num),T(num),H(num),S(num)]<RETURN>

Decrement the block number.

where (num) = 24 bit number (8 bit if T,H,S)

T = first (Hi) byte of block

H = second (Mid) byte of block

S = third (Lo) byte of block

the - command does not decrement properly for H  
and S modifiers

**/** </>[S(num),T]<RETURN>

Choose options (/H for help).

where S = slot set

T = translate current block to  
cylinder/head/sector

**?** Help.

## PART 4 NEW FEATURES

The following new features have been developed since the release of DSKDBG V-E00.16 and are included in DSKDBG V-E00.17.

- \* The Help errors command has been slightly modified. <HE> or <HE1> provides help for the Standard System ROM Z8 and <HE2> returns help for the Format/Debugger ROM Z8.
- \* The Help command lists the form of the extended help commands.
- \* Display now has a command to allow the decoding of the status table into the version, spare list, and bad block list.

DS = display status info.

- \* Use <ESCAPE> or <RETURN> to terminate a long list of spares or bad blocks.
- \* An additional modifier is available for read/write commands that allows you to specify which buffer you are reading to or writing from. For example, a read command followed by >O means read to the output buffer. A write command followed by <I means write from the input buffer.

## PART 5 TYPICAL PROBLEMS AND HOW TO AVOID THEM.

- \* The + (Increment) command doesn't work.

This is to date the most common problem. Usually the command line will look something like

```
R0 PE + X
```

What you were trying to do is sequentially read thru the disk starting at block 0. What you said was

```
Read block 0 (block = 0), Pause on error,  
Increment block (block = 1), Repeat line,  
Read block 0 (block again = 0) .....
```

To fix this problem just do one line to set block 0 and then go on to the next line to do the Read, Pause on error etc.

For example:

```
<R0><RETURN>  
<R><sp><PE><+><X><RETURN>
```

**\* Display Status Won'T Work Or Won't Stop**

The display status command allows you to display the input buffer and make assumptions about what the data means.

For it to work, the Get status command must successfully read the status information from the drive.

If the input buffer has garbage in it, the Display Status command may go round and round trying to display all the spared sectors and bad blocks.

To stop the command when it is caught in a loop or is listing a bunch of bad blocks, simply press the <RETURN> key or the <ESCAPE> key. The functions of the other keys are the same as for all other display commands.

**PART 6 KNOWN BUGS IN VERSIONS E00.17 AND E00.16**

The Macro command has 3 known bugs.

The first occurs when a macro is added to the list and there is already one there of that number. The effect is to make both of them disappear.

The secondbug occurs when the macro is invoked on a line with the X command (eg., M1 X). This disables the <ESCAPE> key so the program can only be halted by re-booting.

The third bug also involves the X command. When a macro is added (eg., R MAl X), it will keep asking to delete the old macro.

The - command doesn't decrement properly for H and S modifiers

## PART 7 STATUS BYTE DESCRIPTIONS

This part provides a bit-by-bit description of the four status bytes available with the Standard System ROM Z8 or the Format/Debugger ROM Z8.

### PART 7.1 STATUS BYTES WITH STANDARD ROM V-3.98 INSTALLED

#### STATUS 1

- 7 = 1 if ProFile did not receive 55 to its last response
- 6 = 1 if write or write/verify was aborted because
  - >532 bytes
  - if data were sent
  - if ProFile couldn't read its spare table
- 5 = 1 if host's data is no longer in RAM because ProFile updated its spare table
- 4 = 1 if SEEK ERROR - unable in 3 tries to read 3 consecutive headers on a track
- 3 = 1 if CRC error (only set during actual read or verify of write/verify, not while trying to read headers after seeking)
- 2 = 1 if TIMEOUT ERROR (couldn't find header in 9 revolutions - not set while trying to read headers after seeking)
- 1 = N/A
- 0 = 1 if operation unsuccessful

(continued on the next page.)

## STATUS 2

7 = 1 if SEEK ERROR - unable in 1 try to read 3 consecutive headers on a track

6 = 1 if spared sector table overflow ( > 32 sectors spared)

5 = N/A

4 = 1 if bad block table overflow ( > 100 bad blocks in table)

3 = 1 if ProFile unable to read its status sector

2 = 1 if sparing occurred

1 = 1 if seek to wrong track occurred

0 = N/A

## STATUS 3

7 = 1 if ProFile has been reset

6 = 1 if block number invalid

\* 5 = 1 if block I.D. at end of sector mismatch

4 = N/A

3 = N/A

\* 2 = 1 if ProFile was reset

\* 1 = 1 if ProFile gave a bad response

\* 0 = 1 if parity error

\* These bits are set by the SOS ProFile driver and are not used by the Dskdbg ProFile.IO.

## STATUS 4

7 - 0 = the number of errors encountered when rereading a block after any read error

1 - 001  
2 - 010  
3 - 011  
4 - 0100  
5 - 0101  
6 - 0110  
7 - 0111  
8 - 1000  
9 - 1001  
A - 1010  
B - 1011  
C - 1000  
D - 1101  
E - 1110  
F - 1111

PART 7.2 STATUS BYTES WITH FORMATTER/DEBUGGER ROM FD3.98 REV  
11 INSTALLED

**STATUS 1**

- 7 = 1 if Profile did not receive 55 to its last response
- 6 = 1 if no index found during formatting
- 5 = 1 if no sector mark found during formatting
- 4 = 1 if SEEK ERROR - unable to read 3 consecutive headers on a track (one try only)
- 3 = 1 if CRC error (only set during actual read or verify of write/verify, not while trying to read headers after seeking)
- 2 = 1 if TIMEOUT ERROR (couldn't find header in 9 revolutions - not set while trying to read headers after seeking)
- 1 = N/A
- 0 = 1 compare error on a write compare

**STATUS 2**

- 7 = 1 if ProFile has been reset
- 6 = 1 if track number invalid while reading or writing a sector
- 5 = N/A
- 4 = N/A
- 3 = N/A
- 2 = N/A
- 1 = 1 if seek to wrong track occurred
- 0 = N/A

(continued on the next page)

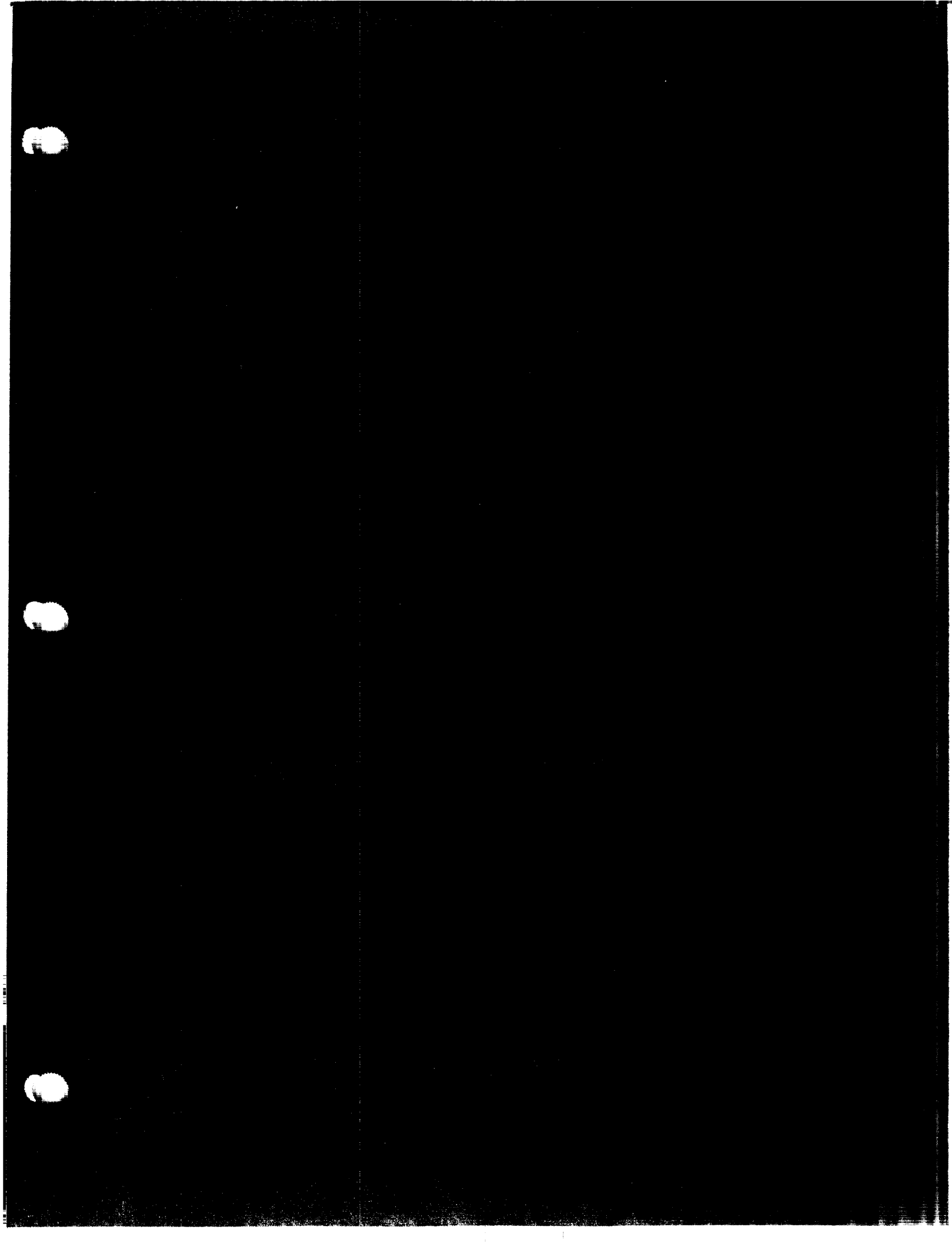
**STATUS 3**

D7, D6, and D5, along with D4 and D3 from STATUS 1, tell why a write compare operation failed.

	D7	D6	D5
write timeout	0	0	0
read timeout	1	0	0
read CRC	1	1	0
data compare	1	1	1

**STATUS 4**

7 - 0 = the number of errors encountered when formatting data fields or scanning the disk.





**SECTION 3**  
**APPENDICES**

**ProFile Service Manual**  
**Section 3**  
**Appendices**

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050-4034, Controller Lisa 2.0	
050-5005, Analog	
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661-92048, Analog	
661-92050, Interface Card	
A9M0005, U.S. Generic ProFile	
A9M1005, Euro Generic ProFile	
A3M0305, ProFile for Apple ///	

## HOW TO USE THIS SECTION

This section contains general information on the functional operation of the 4 modules in the Pro-File, and its firmware operation.

It is designed to be referred to from the other sections in this manual, but you may wish to use it to help you better understand Pro-File operation.

If you are unfamiliar with Winchester disk drives, then a good place to start would be with the Pro-File HDA description in this section.

Then if you would like general information on each of the 4 Pro-File modules read the "Overview of the Pro-File".

## OVERVIEW OF THE PRO-FILE

The following description will give you an overview of the technical details of the ProFile. It is intended to be a summary only, and is not a detailed explanation of the engineering aspects of the ProFile.

### General Information on the Pro-File

The intelligent Controller (Controller PCB), which is built into ProFile is continually checking the operation of the disk. ProFile performs many operations to assure that the user will never see a problem.

These operations start the moment ProFile is turned on. After power-up, ProFile does a Scan operation of the entire disk surface, and checks for any errors.

Upon any data read error, an extensive analysis of the error is performed to determine whether a media error exists. If that is the case, the data will be moved to a spare sector of the disk. That part of the disk with a media error will no longer be used, it is "spared".

In most cases, the error recovery routines in ProFile will be able to extract the data even from a bad sector. The recovery operation includes more than 300 retries under various conditions. Maps of the bad sectors are redundantly recorded on ProFile (these maps are called spares tables), so that an error in the map will not cause a problem in operation.

The ProFile moves the heads to a "parking position" off the data zone after three seconds of no activity. This prevents the loss of data if, for instance, the ProFile is dropped or jarred. ProFile constantly checks for errors during operation.

After any change in tracks, ProFile verifies that the operation has been performed correctly. ProFile also checks that the heads are positioned accurately on a track before any read or write operation is performed.

Unless the system requests that the ProFile do otherwise, data is always verified after a write operation. In all these cases, ProFile will correct the problem so that no errors occur.

Data can be transferred from the ProFile to the system at up to one Mbyte per second DMA rate. Data is interleaved at a 5:1 ratio, which allows three 512 byte sectors to be transferred on each rotation. MFM encoding allows the maximum data storage capacity with low formatting overhead.

- Note:**
1. For more detailed information on Scan operation, and error recovery routines refer to the firmware routine's functional description in this section.
  2. For more information on the format (including spares tables), used for the Pro-File HDA refer to the Pro-File HDA description in this section.)

### **What is ProFile?**

ProFile is a Winchester technology hard disk drive designed to operate with a host computer. It has a formatted storage capacity of 5 Megabytes, which is essentially the same as 35 floppy disks (the Apple III disk drive uses floppies that have a capacity of 140K Bytes).

Functionally, the ProFile consists of four major modules:

1. The Controller PCB
2. The Analog PCB
3. The Power Supply
4. The Hard Disk Assembly (HDA) with motor control PCB

The discussions on the following pages describe the general function of these modules.

## 1. The Controller PCB

Functionally, the Controller provides communications with the host computer, provides signals to read and write serial data on the disk, moves the heads to the proper track, and monitors error conditions.

The Controller consists of a Z8 microprocessor, 2K bytes of RAM, error detection logic, and read/write control logic.

The Z8 provides an intelligent interface to the host computer. High level commands, such as read, write, and status, are generated by the host computer to through the Pro-File interface cable to the Z8. The Z8 uses the buffer area in RAM to temporarily store any data being read from or written to the disk.

The Controller also interfaces to the Analog card to pass head control information to it. In this way the Controller determines when read/write operations will take place.

The Z8 controls disk operations in the HDA. Basically it sends the stepper motor in the HDA step pulses to move the heads from track to track (such moves are called "seeks"), selects one of four read/write heads, and enables the different functions (i.e. sync, clock data, etc.) on the Analog PCB to perform the read or write operation called for by the host.

Read/Write functions are performed by the read/write logic on command from the Z8. This logic in turn controls the parallel to serial data conversion when writing, and the serial to parallel data conversion when reading.

To ensure the proper transfer of data, the Controller does a CRC (cyclic redundancy check) of the serial data. If an error occurs, the Z8 will automatically perform an error recovery routine and try to relocate the data onto a different section of the disk. The sector causing problems will be removed from use to prevent future errors.

After 3 seconds of no communication with the host, the Z8 on the Controller PCB will move the head to a Park position on the disk (track 155 a non data track), to prevent accidental damage to the disk surface in the event of a hardware failure (such as power loss). Once in Park position for 0.75 seconds, the Z8 removes power from the stepper motor to prevent heat build-up in the drive.

The READY light on the front of the ProFile is lit whenever the Controller is idle (not busy).

## 2. Analog PCB

The Analog PCB serves as the interface between the Controller and the Head Disk Assembly (HDA).

The Analog PCB consists of a data encoder, a data decoder, write driver, head select logic, automatic gain control (AGC) preamplifier, read detector, phase lock loop (PLL), and sector detector.

The head select matrix selects one of the four heads for a read or write operation in response to control signals from the Z8 on the Controller PCB.

The ProFile has two fixed disks in its HDA, and there are two heads for each disk (one for each side, since the disks are double sided). Thus you have a choice of four heads, depending on which section of the disk you are trying to access.

It is not necessary for the host computer to know which section of the disk it is trying to access; the Controller and the Analog PCB take care of that.

During a write operation, the serial data is encoded using a technique known as Modified Frequency Modulation (MFM).

During a read operation, the AGC circuit amplifies the low level head signal (.6 to 2.0 mv) to a fixed signal level (1.0 volt). The read detector simply shapes the signal so that it appears in a standard fashion.

The PLL and data decoder then convert this signal back into serial data, which is passed to the Controller, which in turn converts it to parallel data and passes it to the host computer.

High speed, low noise ECL (emitter coupled logic) provides wide margins for the Analog electronics PCB of the ProFile.

When the disk is initially formatted, the sector boundaries are written to the disk (this is done by removing all read signals from certain sections of the media). During the read operation, the sector detector looks for these areas of no read signal, and signals the Controller that a sector boundary has been found.

### 3. Switcher Power Supply

The power supply provides the +5VDC, and +12VDC needed by the ProFile for operation.

The supply also contains monitoring circuitry to detect a power failure. This monitoring circuitry senses a power failure before the internal DC voltages drop.

If a power failure should occur the monitoring circuitry uses a signal called Power OK (POK) to reset the Z8 on the Controller PCB.

This allows the intelligent Controller in ProFile to prevent any data loss if the power fails or is turned off accidentally. The system will not begin any operation until the power is on for at least one second.

Once a failure is detected, the head current is shut off to prevent the accidental writing of false data that would otherwise occur if a write operation were in process when the power failed. The power supply is completely shielded to eliminate the effects of electro magnetic radiation.



#### 4. Head Disk Assembly (HDA)

The ProFile HDA is a random access storage device with two non-removable 5 1/4 inch discs as storage media. Each disk surface employs one movable head to service 153 data tracks. The total formatted capacity of the four heads and surfaces is approximately 5 Megabytes (16 sectors per track, 512 bytes <A/// format> or 532 bytes <Lisa format> per sector, and 612 tracks).

High reliability is achieved through the use of a band actuator and open loop stepper head positioning mechanism. The read/write heads are mounted on a ball bearing supported carriage which is positioned by the band actuator connected to the stepper motor shaft.

Mechanical and contamination protection for the heads, actuator, and discs are provided by an impact resistant aluminum enclosure. A self contained recirculating system supplies clean air through a 0.3 micron filter.

A special spindle pump assures adequate air flow and uniform temperature distribution throughout the head and disk area.

Thermal isolation of the stepper and spindle motor assemblies from the disc enclosure provides significantly greater "off track" margin (temperature changes are less likely to cause read errors).

A brushless DC drive motor rotates the spindle at 3600 RPM. The spindle is driven directly with no belt or pulley. The motor and spindle are dynamically balanced to insure a low vibration level.

Depending on the revision of Motor Control PCB on the HDA a physical brake mechanism, or a dynamic brake (involving reverse biasing the coils on the disk motor) may be used to provide a fast stop to the spindle motor when power is removed. (continued on the next page)

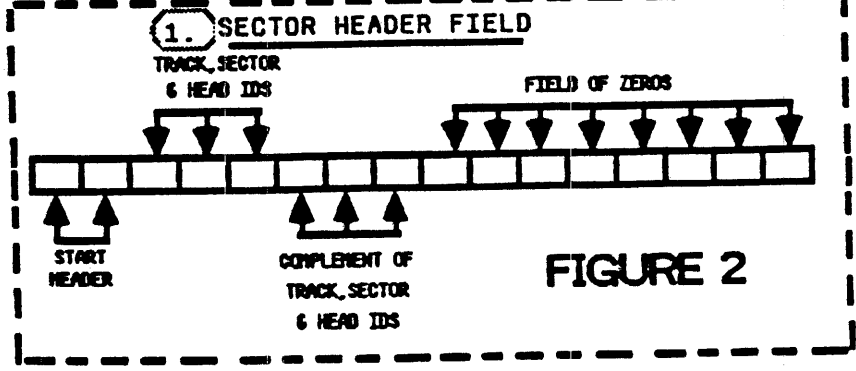
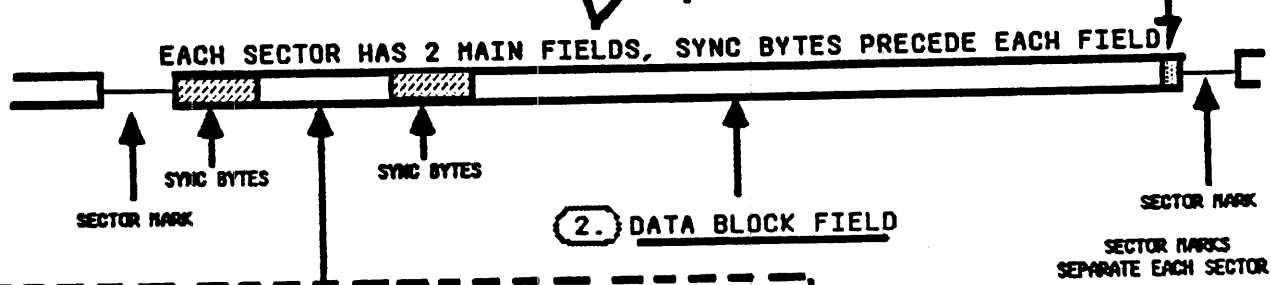
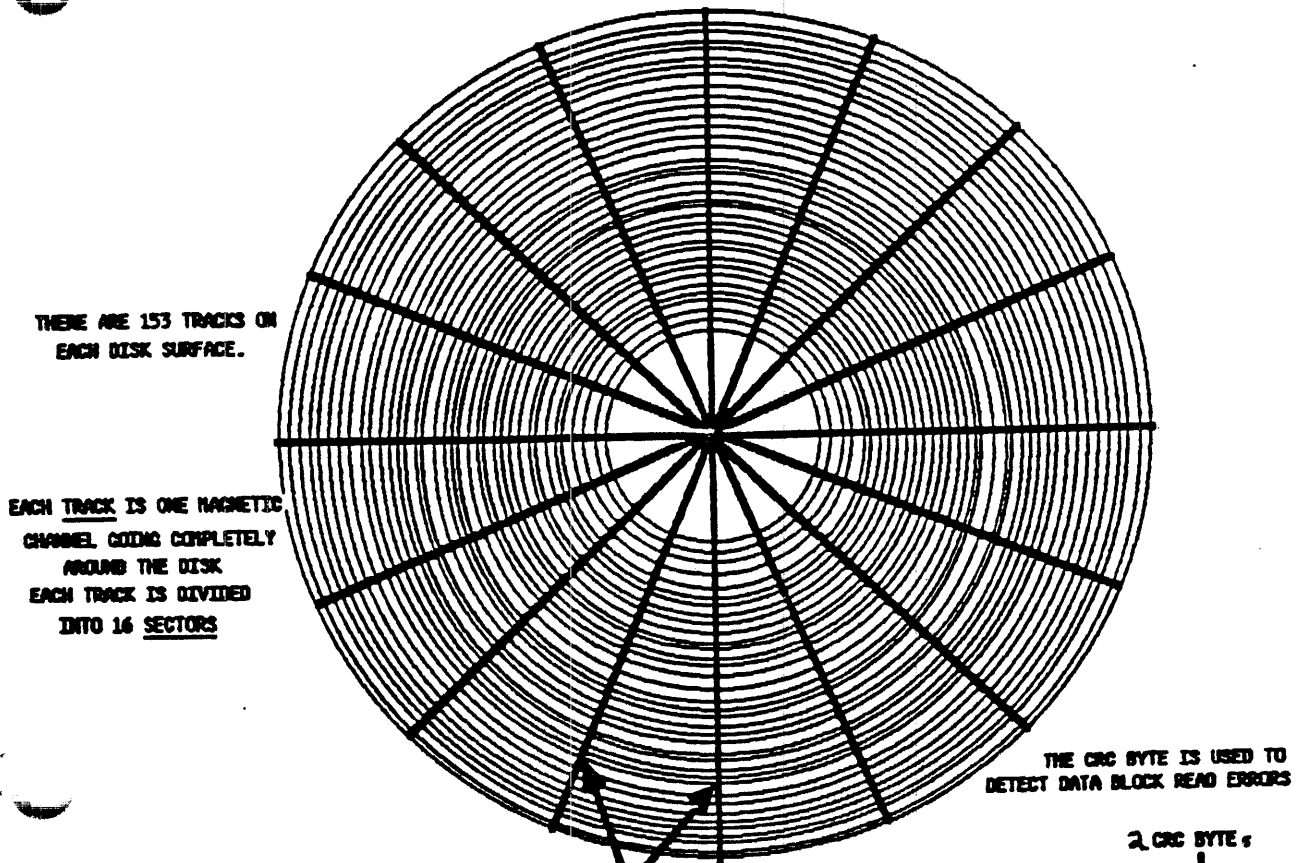
#### 4. Head Disk Assembly (HDA) (continued)

The recording media consists of a lubricated thin magnetic oxide coating on a 130 mm diameter aluminum substrate. This coating formulation, together with the low load force, low mass Winchester type "flying heads", permits reliable contact start/stop operation.

The HDA (hard disk assembly) can be operated from 10°C to 60°C/. This wide operating range, combined with a 75% efficient switching power supply allows ProFile to operate from 10 to 40°C in still air without a fan.

(For more information on the Pro-File HDA format (including spares tables), used for the Pro-File HDA refer to the Pro-File HDA description in this section.)

**FIGURE 1**



**FIGURE 2**

PRO-FILE HDA DESCRIPTION  
(THE HARD DISK ASSEMBLY)

PHYSICAL DESCRIPTION OF THE HDA

The HDA contains 2 rigid disks, which are constantly rotating at 3600 RPM. Each disk has 2 surfaces, (top and bottom), making a total of 4 surfaces numbered 0, 1, 2, and 3 (see figure 1).

The disk surfaces are covered with a metallic film which is very easily magnetized. In the beginning, when the disk is first made, there is no magnetic information on it at all.

No information will be put on the disk until its magnetic areas have been specially arranged, or **formatted** with a Format program run from the Host computer system. A discussion of the features common to formats used for the Pro-File HDA is explained later in this discussion.

Each surface has a device called a head, which converts electrical impulses into magnetic impulses and vice versa. The heads are numbered after the surfaces they cover, that is, 0, 1, 2, and 3.

During a write operation, binary data in the form of a bit stream is written on the disk surface by the head. As the disk surface rotates under the head, each pulse in the bit stream will cause a small area on the medium (disk surface) to be polarized.

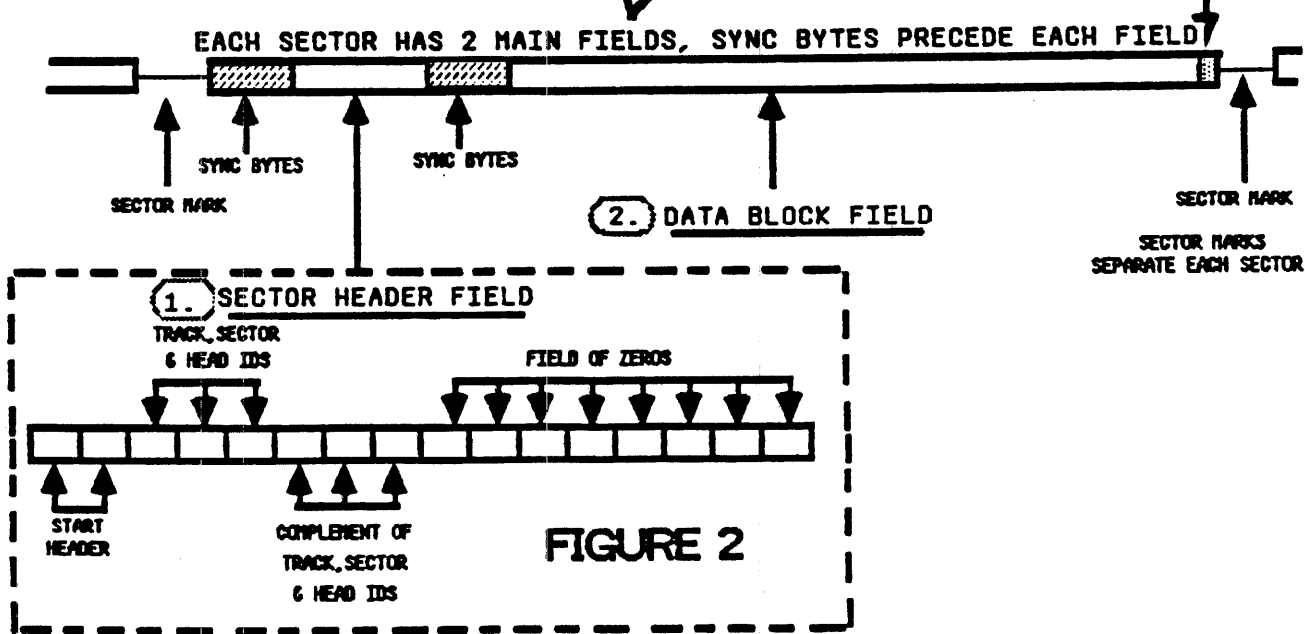
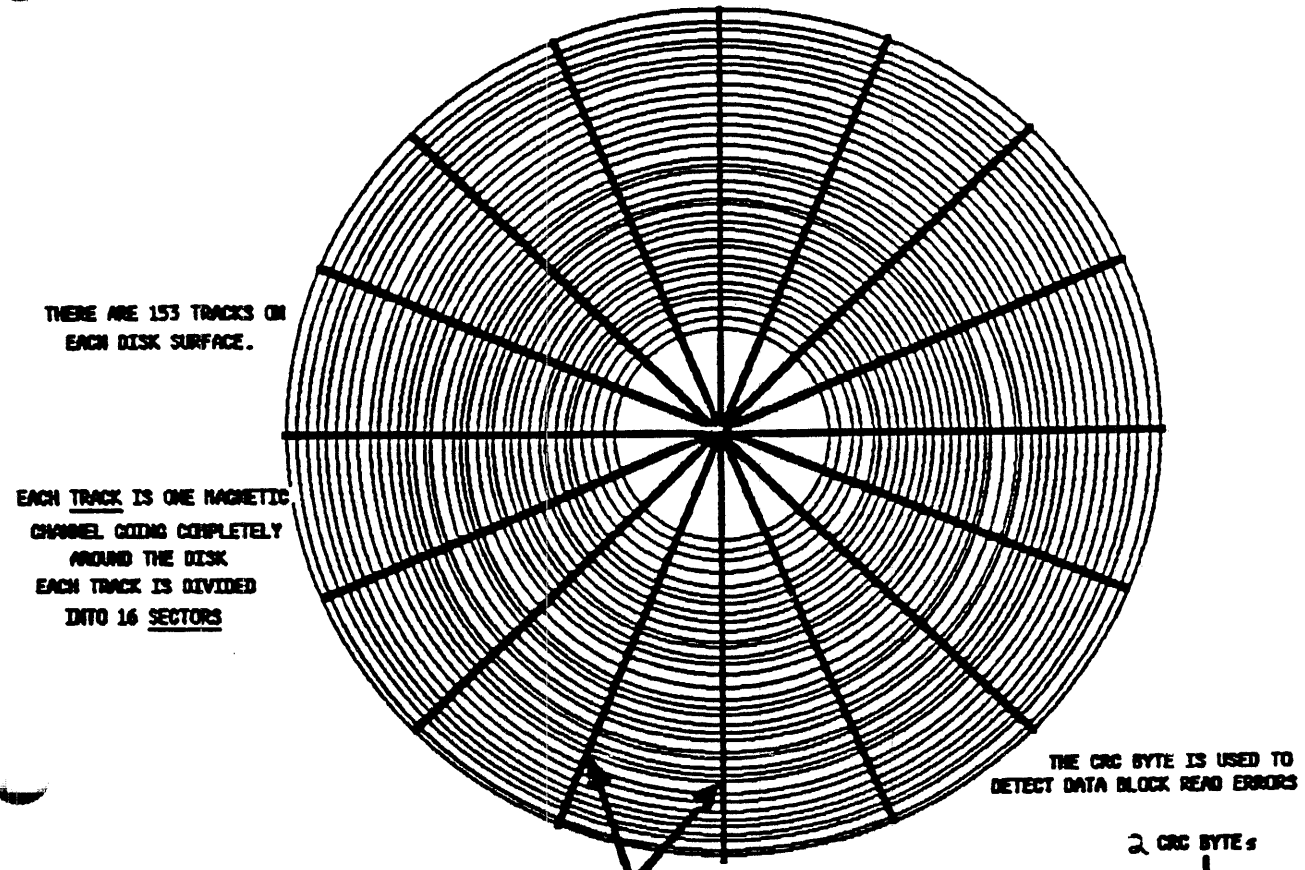
Extreme closeness of the head to the medium (in the Pro-File's case 20 microinches) is a distinguishing characteristic of Winchester type disk drives.

The head rides (flies) on the thin cushion of air between it and the media (something like an airplane wing). If particles as small as a piece of dust are allowed into the head chamber, they can cause the head to lose its flight stability. The head may then become erratic causing it to crash into the media, and destroy some areas on the disk.

For this reason, the HDA is kept in an air-tight enclosure with a small filtered aperture. This allows atmospheric pressure equalization while preventing potentially dangerous particles from gaining access.

During a read operation, the head senses the magnetic areas on the disk surface as they pass under the head, and produces an electrical impulse for each change in their polarity.

**FIGURE 1**



## DESCRIPTION OF THE PROFILE HDA FORMAT

Now you know how binary data is written onto and read from the disk. But how does the drive store different sets of data (files) and keep them separate?

To do this, the drive needs a way of writing different files to different areas of the disk, and then finding them when it needs to read them.

To understand how the drive does this, you need to understand **steps, tracks, blocks, and sectors.**

Each head is mounted in such a way that it may move in to the center and out to the perimeter of the disk surface as the disk rotates beneath it.

A write or read operation will never take place while the head is moving, but only while the head is stationary and the disk is moving under it.

The heads move in very exact increments called **steps**. On the Pro-File the head must take 153 steps to cover the entire area on the disk where data may be stored. The head may stop after any step to read or write data. The 153 possible positions of the head determine the 153 magnetic channels, or **tracks**, on which data can be stored (refer to figure 1).

The selection of which track the head is positioned over is controlled by the firmware program in the ROM on the Z8 microprocessor on the Controller PCB (the particular firmware routine used for this purpose is called the **Seek Routine** and is discussed in the Firmware Routine descriptions in this section).

The Z8 performs track selection by sending step pulses to the motor controlling the head. The number of step pulses the Z8 sends to the stepper motor determines how far the head will move and so which track it will be over.

## DESCRIPTION OF THE PROFILE HDA FORMAT (continued)

The firmware program in the Z8 also controls when a read or write operation occurs. When writing, the bit stream to the head travels from the Host (Apple ///, or Lisa), to the Pro-File's electronics, to the head; and when the bit stream is read from the disk it goes back to the Pro-File's electronics, and then to the Host.

There are 612 tracks on the HDA (153 tracks on each disk surface, and 4 disk surfaces), and approximately 8,200 bytes on each track.

If track selection were the only method the Z8 firmware had to control the location of stored data, it would have a maximum of 612 very large storage places (8,200 bytes apiece). Since most files are considerably smaller than 8,200 bytes, this would be very inefficient.

So to make data storage more efficient, the host computer breaks all data up into segments called **data blocks**. If the Host is an Apple /// the data blocks are 512 bytes long, and if the Host is a Lisa they are 532 bytes long.

The Pro-File stores these **blocks** into physically addressable areas on the track called **sectors**. There are sixteen sectors on each track (refer to figure 1), so each track on the Pro-File can hold 16 data blocks.

The sectors are separated from each other by small blank areas of no writing called **sector marks**. The Pro-File uses these sector marks to detect when one sector ends and a new one begins.

Each sector can be divided into 2 fields: the first field is called the **sector header**, the second field follows the sector header and is called the **data block** (see figure 2).

(Continued on the next page.)

## DESCRIPTION OF THE PROFILE HDA FORMAT (continued)

Each field in the sector is preceded by sync bytes to allow the Pro-File electronics to synchronize to the data in the field before attempting to read one.

The sector header field contains 16 bytes: 2 are "start header" bytes; 3 bytes contain track, sector, and head ID's; 3 bytes contain a complement of the track, sector, and head ID information; and the remaining 8 bytes are all 0's.

The data block field consists of the actual data from the Host computer with 2 CRC bytes at the end (a CRC (Cyclic Redundancy Check) byte is used by the Pro-File electronics to detect if an error has occurred during a read or write operation).

The data block field is transparent to the Pro-File (which can only locate sectors), so the operating system from the host computer must keep track of which data block is in which sector.

The operating system references sectors by block numbers. It knows that it has 9728 (decimal), or 0 to 25FF (hexidecimal) sectors available for data on the Pro-File.

So it assigns each block of data to a number from 0 to 25FF called its **logical block number** and writes/reads the data blocks to/from the Pro-File using this number. The Pro-File converts the **logical block number** into sector locations to actually store or read the data block.

During formatting, the Format program writes the sector marks and headers into their areas within each sector. At this time, all sectors are referenced to a physical location on the disk called the Index (see figure ).

The Index position is sensed when a small magnetic tab fastened on the disk motor passes by a magnetic sensor during motor rotation.

Note: The Index signal is only used during formatting, although it may be sampled by the technician with a frequency counter to determine the HDA's motor speed.

(Continued on the next page.)



## DESCRIPTION OF THE PROFILE HDA FORMAT (continued)

In a properly operating Pro-File, sector marks and headers should never change after formatting, since the locations of the sectors will never change. A data block, on the other hand, will change every time its file is written to, by the Host computer system.

When looking at figure you probably noticed that the sectors are not sequentially numbered. This is because the sectors are **interleaved**. When the Pro-File goes after a sector, it reads sector headers to determine where the head is in relation to the target sector.

Without **sector interleaving** if it read the sector header of the sector immediately preceding the target sector, then the electronics in the Pro-File could not react fast enough to begin reading the data block of the target sector, so it would have to wait another complete revolution of the disk to do so.

With **sector interleaving** the program can read a sector header and know that the next sector in the numerical sequence will always occur a specific number of sectors following it, so it has time to prepare within that same revolution.

**Sector interleaving** is a result of the formatting for a given system. The format in the figure shown is for an Apple /// system. Each sector in this format is offset from the next in its numerical sequence by 5 sectors. The interleaving scheme for a Lisa system offsets the numerical sequence of each sector by 7.

## SPECIAL FUNCTION TRACKS

**Directories:** Now another question: How does the host computer's operating system keep track of where all the blocks belonging to a file are located?

The answer, it uses the Pro-File's HDA to store **directory** information on each file.

Directories are created and maintained by the host computer's operating system. As far as the Pro-File is concerned, they are just data block fields. But without them the operating system would not be able to send the Pro-File the proper block numbers to retrieve the data blocks for a file.

**NOTE:** The following discussion which very briefly describes the Apple /// Sophisticated Operating System's (SOS) directory usage, is for example purposes only, and subject to change as the Sophisticated Operating System is revised.

On an Apple /// system, track 0 on the Pro-File is reserved for the **Root directory** which contains descriptive information about every main file that SOS (the Apple /// operating system) has put on the Pro-File. This information includes:

- a. File name - The name of the file in ASCII.
- b. The block number for each file's key block - Each file's key block contains many items of information about the file. Among them will be a list of every block number in the file.

When an Apple /// host computer wants a file it reads the Root directory which refers it to the file's key block (this may be through several subdirectories). The host then reads the key block and sequentially takes each block number from the file's block listing in the key block and sends it to the Pro-File to read the file.

The firmware program in the Z8 takes care of converting the logical block number from the host to a sector address so it can actually acquire the data block. (For more information on the Apple /// directory structure refer to the SOS Reference Manual)

## SPECIAL FUNCTION TRACKS (continued)

A Lisa uses a different directory structure, but Pro-File operation is still the same.

Because all communication between the Pro-File and the HOST is done block by block, the Pro-File is known as a **block device** (as opposed to **character devices**, which communicate one byte at a time (such as a printer)).

The next block in the file is not necessarily located in the next sequential sector on that track. In fact very often it is located on an entirely different track.

That is why the Pro-File sometimes seems to go through a lot of gyrations as it reads a file. The sectors containing the blocks in the file are probably located on several different disk surfaces and tracks.

Track 77 on all disk surfaces is dedicated for the exclusive use of the Pro-File. The host cannot write to these tracks unless the Pro-File is being formatted. The following discussion describes their usage.

### The Spares Storage Track (Track 77, Disk Surfaces 0, and 1): What happens if there is an error?

When the Pro-File looks for a block of data, it performs many tests to confirm that the correct sector is being read accurately (for a more detailed description of these tests, refer to the Firmware Routines description in this section).

Sometimes the Pro-File determines that the media where a sector is located is not useable, and so won't use it any more. A sector identified as being unuseable is called a **spared sector**.

If the data block from the spared sector can be salvaged, the Pro-File will store the data block from the faulty sector on a special track reserved for that purpose called the **Spares Storage Track** (located on track 77 on disk surfaces 0 and 1).

## SPECIAL FUNCTION TRACKS (continued)

The **Spares Storage Track** provides storage for a maximum of 32 spared sectors (2 surfaces, 1 track on each surface, 16 sectors per track).

**The Spares Table Track (Track 77, on Disk Surfaces 2, and 3):**  
Once the data block from the spared sector has been stored, the Pro-File will record the old sector location of the salvaged data block along with its new spares storage sector location in the **Spares Table Track** (located on track 77 on disk surfaces 2, and 3).

Spares table information is stored redundantly on the **Spares Table Track** so any addition of a newly spared sector address will require an update to all 32 sectors on both surfaces of this track.

When the host sends the Pro-File a block number to be read, the Z8 will search the **Spares Table** (an image of this table is maintained in RAM), to determine if that block is on the **Spares Storage Track**. If it is, the Z8 will then go to the spares sector address to acquire the data block.

## FIRMWARE ROUTINES

The following descriptions discuss the operation of some of the firmware routines contained in the ROM of the system Z8 on the Controller PCB, and how they affect the operation of the Pro-File.

### 1. SCAN OPERATION

After power up there are several things that take place before the firmware program in the system Z8 microprocessor on the Controller PCB will allow communication with the host computer system.

**Note:** The position of the heads over the disks may be visually monitored by observing the position of the Interruptor arm on the HDA (as shown in Sheet 1 of the troubleshooting flowchart).

- a. **First** the power must come up to the proper levels and be stabilized. **Note:** To indicate this process, upon power up, the Ready Lamp will light for between 0.5 and 3 seconds.
- b. **Second** the Z8 waits for about 20 seconds to allow the HDA motor to come up to 3600 RPM (its operating speed). **Note:** During this process, the Ready Lamp will remain off.
- c. **Third** the Z8 does a **Seek** routine to the **Spares Table Track** on track 77, on disk surfaces 2, and 3. **Seek** routine operation is standard for any read, write, or write/verify operation requiring head movement to a new track and is performed as follows.

During the **Seek** routine the Z8 issues the proper number of steps to the stepper motor to move the head over the target track, and performs a verification process to confirm that the head is over the proper track.

During the **Seek** verification process the Z8 reads 3 alternate sectors from the track the heads are over.

(Continued on the next page.)

## 1. SCAN OPERATION (continued)

The sector header fields from these sectors tell the Z8 which head and track have actually been selected. A CRC check is also performed on the data block fields from these 3 sectors.

- (a) If the head and track ID's read from the 3 sector header fields prove that the proper head is positioned over the proper track, and the 3 data block field's CRC status is OK, then the Z8 will exit the Seek routine and enter the Read routine.

The Read routine would normally read every sector on the now confirmed track until the target sector is read. However since each sector on the spares table track is redundant (each sector contains the duplicate copies of the spares table), there is no target sector.

Any sector that has a good CRC check during read is acceptable. If the first sector has a CRC error, then the Z8 will just read the next and so on until it finds a good one.

- (b)\* If during the attempt to confirm a good Seek to the Spares Table Track on track 77, a sector header is unable to be read, or a CRC error in a sectors data block field occurs, then the Seek routine will continue reading the 3 alternate sectors for up to 64 errors.
  - \* If over 64 errors occur, then the Z8 moves the head to track 0 (the outermost track) and tries the Seek routine to the target track again (in this case track 77). If that fails the Z8 will move the head in to track 155 (the innermost track) and again reseek to the target track.
  - \* The head movement to track 0 and track 155 and reseeking process during Seek verification is performed twice.

If the proper track is still not found, then the Seek routine will be exited, Scan operation is abandoned, and the heads are moved back to park position.

(Continued on the next page.)

## 1. SCAN OPERATION (continued)

- d. **Fourth** the firmware program in the Z8 performs a sector header read, and data block CRC check of every sector on the HDA beginning with track 0 as follows: **Note:** The Ready Lamp will flash on and off during this process.

- (1) Each movement of the heads to a new track requires a **Seek** routine as described above.

- (a) If the head and track ID's read from the 3 sectors during the **Seek** routine prove that the proper head is positioned over the proper track, and their CRC status is OK, then the Z8 will exit the **Seek** routine and enter the **Read** routine.

The **Read** routine will read each sector header on the track until it finds one that matches the target sector whose sector address is currently in RAM.

- \* If during the **Read** routine the correct header is found, then the data block is read and its CRC status is checked. If the data blocks CRC status checks good, then the Scan operation goes on to the next sector to be read.

- \* If during the **Read** routine there is a timeout error (the target header cannot be found within 150 ms), or a CRC error occurs in the target sectors data block field, then the **Retry** routine (described in section 2) is called to attempt to get a good data block read from the sector.

- (b) At this point in **Scan** operation, if an error occurs the **Seek** error recovery procedure described above will be followed, with the following exception.

If after the procedure is accomplished the proper track is still not found, then the Z8 will use the last track it could confirm a good seek on, as a reference to approximate the position of the target track, and move the head to that position. Then regardless of whether it could confirm a good seek to the target track or not, it will exit the **Seek** routine and enter the **Read** routine to read the target sector.

## 2. RETRY ROUTINE

The Retry routine is called for the purpose of attempting to read a good data block field after an unsuccessful read operation has occurred.

There are 2 variables in the Retry routine, the retry number, and the sparing threshold. These values are given by the host computer's operating system when communications between it and the Pro-File are initiated.

During the Scan operation since no communication from a host can occur, default values of 105 for the retry variable, and 31 for the sparing threshold are used. When called the Retry routine will:

- a. Read the target sector the number of times specified by the retry variable (in the Scans case the default value is 105)
  - (1) If after the total number of retrys have occurred, there are no successful reads, the Retry routine will try to reread the sector 90 more times, or until it reads a data block without a CRC error.
    - (a) If all of the 90 reads are unsuccessful, then the sector address is written to the bad block table in RAM, and the spares table track (track 77 of disk surfaces 2 and 3).

**Note:** If Retry is called during Scan operation, the spares table track (track 77 on disk surfaces 2 or 3) will be updated when the host computer's operating system initiates communication with the Pro-File (this will be after the completion of Scan).

- (b) If any of the 90 reads are successful a good data block from one of the successful reads is held in RAM while the Diagnostic routine (described later) is called to check out the media for the sector in question. If the Diagnostic routine determines that the sector has bad media, it will spare the sector. If the Diagnostic determines the sector to be good, then the Diagnostic and Retry routines are exited.



## 2. RETRY ROUTINE (continued)

(2) If after the total number of retries have occurred, there were successful reads, then the Z8 checks to see if there were more unsuccessful reads than the spares threshold variable allows (in Scans case the default is 31).

(a) If the sparing threshold has not been exceeded then the Retry routine is exited, and control is given back to the Scan operation.

(b) If the sparing threshold is exceeded, but at least 1 good data block read occurred, then the data block field is rewritten to the questionable sector and the Diagnostic routine (described later) is called to check out the target sectors media.

If the Diagnostic routine determines that the sector has bad media, it will spare the sector. If the Diagnostic determines the sector to be good, then the Diagnostic routine is exited and control is given back to the Scan operation.

### 3. DIAGNOSTIC ROUTINE

The Diagnostic routine is called for the purpose of checking media quality on a given sector location, and sparing the sector if the media quality is determined to be bad. When the Diagnostic routine is called it will:

a. Read the target sector (specified by the sector address currently in RAM), 100 times.

- (1) If over 30 CRC and/or timeout errors occur, then the Diagnostic routine will write the data block into a sector on the spares storage track (track 77 of heads 0 or 1).

The Diagnostic routine will then write the old sector address, and its new spares track sector address in the spares table in RAM, and after the next handshake with the host system will update the spares table track (track 77 on heads 2 or 3).

The Diagnostic routine is then performed on the new spare sector location of the data block to make sure that it is a good media location.

**Note:** During Scan operation the spares table track (track 77 on disk surfaces 2 or 3) will be updated when the host computer's operating system initiates communication with the Pro-File (this will be after the completion of Scan).

- (2) If less than 30 CRC or timeout errors occur, then the Diagnostic routine is exited, leaving the data block in its present sector (the media must be OK).

**4. During Normal Operation** - the Seek and Read routines will be performed just as they were in the Scan operation.

If an error occurs, the sequence of operations is the same as that of scan with the exception that the retry and spares threshold variables will be different depending upon the operating system.

The Diagnostic routine will always be called if the verify fails during a Write/Verify operation.

If a sector address is in the Bad Block table, then that means that a Retry routine must have been called for that sector, and during the routine there was never a good read of the data block.

This means that the Pro-File does not have a good data block for that sector and can't perform a Diagnostic on the questionable sector location until it has one.

If the host does a write to that sector address listed in the Bad Block table, then at that time the Pro-File has a good data block for that sector so then the Diagnostic routine is automatically called to verify the media at that location.

Of course if it doesn't check out then the sector is spared. In any event, whether the sector is spared, or is determined to be good and left as is, the sector's address will be deleted from the Bad Block table because the Pro-File now knows whether its media is good or not.

CONTROLLER PCB CIRCUIT DESCRIPTION

**What's in This Description**

On the next six pages you will find tables listing the pins and their functions for the:

- a. Host interface plug P1.
- b. Analog PCB interface plug P2.
- c. Z8 Main Processing Unit on the Controller PCB.

Block diagram and circuit descriptions for the main functions on the Controller PCB follow these tables.

For specific circuit diagram information refer to the Controller PCB schematic at the end of this section.

**Controller PCB to Host Interface (P1)**

The Controller PCB and the Host communicate via a 25 pin plug, P1. Signals at P1 on the Controller PCB are as follows:

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
5, 6, 8, 11 12, 13 22, 23	XD0-XD7	(bidirectional) /Data lines between the Host and the Pro-File.
3	RRW	(input) /Controls the direction of data on lines XD0-XD7.
17	CMD	(input) /Initiates communication with the Pro-File.
16	BSY/INT	(output) /Notifies the Host of Pro-File status.
15	PSTRB	(input) /When writing, this signal is generated by the Host to clock a byte into Pro-File's RAM; when reading, the pulse causes the Z8 to increment the Address Counters and so select the next sequential address to be read. During Read, the RAM is always selected to output the contents of the selected address; so after the Host generates PSTRB, it waits a short time and then gates in the byte from the I/O cable.
18	TPARITY	(output) /This signal is high or low, depending on the parity of the byte currently being transferred on data lines XD0-XD7.
21	CRES	(input) /When generated by the Host, this signal resets the Z8 to its initial state. This usually occurs at the beginning of communications, but whenever it happens depends on the Host.
25	CDET	This signal is used by Host interface to detect a disconnected or broken cable.
1	PHO	(input) /PHO is a timing signal from the Host.

## Controller PCB Circuit Descriptions

### Controller PCB to Analog PCB Interface (P2)

The Controller PCB and the Analog PCB communicate via P2. The Analog PCB converts the Controller PCB's digital data into analog signals for the disk media. Signals at P2 on the Controller PCB are as follows:

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
12	Write Data	(output) /NRZ serial data to be written on the disk.
32	Read Data	(input) /Digitized NRZ serial data recovered from the disk.
10	Sys Clock	(output) /Provides the 10 MHz system clock to the Analog PCB for write operations.
34	Read Clock	(input) / Provides the Controller PCB with a clock that is in sync with the Read data.
30	Read Gate	(output) /Enables the Read circuitry on the Analog PCB.
22	Write Gate	(output) /Enables the write circuitry on the Analog PCB.
4	Index	(input) /Index is a pulse that occurs once per disk revolution and is only used by the Z8 during formatting.
8	Write Sector Mark	(output) /Enables the Analog PCB to write DC sector boundaries during formatting.
15	Sector Mark	(input) /Signals the Controller PCB when the heads have encountered a sector mark on the disk.
26, 28	Head Select 1,0	(output) /Causes selection of one of four Read/Write heads.
2	Track 0	(input) /Indicates that the heads are positioned over the outermost tracks.
24	Precompensation	(output) /Enables the Precompensation and low current circuitry on the Analog PCB when the inner tracks (128 to 152) are being written to.
14, 16, 20, 18	Stepper Phases	(output) /Activates stepper motor coils to position heads. Generated by the Z8.

## 28 Main Processor Pin Descriptions

The following are signal descriptions produced from the Z8 on the Controller PCB. The Z8 has five sets of pins:

1. General purpose signals.
2. Port 0.
3. Port 1.
4. Port 2.
5. Port 3.

### 1. General Purpose Signals

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
2, 3	Clock	5 MHz
6	Reset	'Power OK'; system reset line or $\overline{\text{CRES}}$ .
9	$\overline{\text{AS}}$	Address strobe, used to latch data from Port 1 and Port 0 [0:3] into LS161 counters (RAM address counters).
8	$\overline{\text{DS}}$	Data strobe, defines data valid time during Writes or Reads to RAM and writes to 8253 counter.
7	$\overline{\text{ZRW}}$	Z8 Read/Write line. Defines external memory for I/O operation as a Read or Write.

NOTE:  $\overline{\text{AS}}$ ,  $\overline{\text{DS}}$ , and  $\overline{\text{ZRW}}$  are tri-stated when Port 1 is placed in the high impedance state.

### 2. PORT 0

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
13,14 15	P00-P02 A8-A10	High-order address bits, A8-A10, for RAM access. They are latched into the LS161 address counter during AS.
16	P03 PCOMP	Precomp/Reduce Write Current command to disk Write electronics. (State is 'don't care' if not writing.)
17,18 19,20	P04-P07 01-04	0B2, 0B1, 0A2, and 0A1 commands, respectively, to the stepper motor drive circuitry.

## Controller PCB Circuit Descriptions

### 3. PORT 1

System data bus (8 bits). Its different functions are listed below.

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
21 thru 28	P10-P17 ZR7-ZR0	a. Low order address bits and data, multiplexed by AS and DS, for Z8 RAM accesses.  b. Data bits for loading the 8253 counters. (LDCTR, derived from DS when MSEL1 is low, is the 'Write' input to the 8253.)  c. Data to 1 from the Host. The Z8 program must set Port 1 to the high impedance state.  d. Data to 1 from the disk. The Z8 program sets Port 1 to hi-Z.

### 4. PORT 2

These pins are programmed as inputs or outputs using a Z8 mode register. All pins are set to hi-Z (input mode) after a reset.

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
31	P20 WRTSM	Write Sector Mark (WRTSM) output. This signal, used in conjunction with Format Enable (FMTEN), which causes WTGT to be true, writes sector marks on the disk. This should happen only during the format operation.
32	P21 TRK0	Track 0 (TRK0) input. Indicates that R/W heads are positioned over outermost track.
33	P22 CMD	Command (CMD) input. This line is set true by the Host via the interface card, and it indicates that the Host is requesting access to the controller RAM. The corresponding handshake line, BSY/INT, is a Z8 output described later.
34	P23 BSY/INT	Busy/Interrupt (BSY/INT). This signal acknowledges the CMD input via the CMD-BSY protocol described elsewhere. BSY can also be used to interrupt the Host if enabled on the Interface card.

(Continued on the next page.)



(Port 2 pin description is continued from the previous page.)

- 35     **P24**         (MSEL0) The low order select bit to control  
          **MSEL0**         RAM access.
  
- 36     **P25**         (MSEL1/PSEL) High order RAM access select  
          **MSEL1**         bit. Also controls data input to RAM from the  
                          Host or the disk; hi = disk, low = Host.
  
- 37     **P26**         Start/reset error (START/RSTERR). Enables  
          **START/**         Read/Write control hardware to begin a Read  
          **RSTERR**         or Write operation at the next sector  
                          pulse. Also resets the CRC error flip-flop  
                          and the sector timing register.
  
- 38     **P27**         Disk Read/Write (DRW). Controls the Read/  
          **DRW**             Write inputs to the RAM for Host or disk  
                          accesses. Command input to Read/Write  
                          hardware. High when Read, low when Write

**5. PORT 3**

P33-P30 are inputs and/or interrupts; P37-P34 are outputs.

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
5	P30 SER IN	Not currently used.
39	P31 SECTOR	This signal is generated on the Analog PCB whenever it detects a Sector Mark on the disk.
12	P32 SECTDN	Sector Done (SECTDN). (Input) Resets the 8253 byte counters and the lower four bits of the RAM address counter when the Read/Write hardware is searching for the target sector. Goes low when the Read/Write operation has been completed. Stays low until START.

(Continued on the next page.)

## Controller PCB Circuit Descriptions

(Port 3 pin description is continued from the previous page.)

- |       |                    |   |
|-------|--------------------|---|
| 30    | P33<br>CRCERR      | CRC Error (CRCERR). (Input) Goes low if a CRC error is detected during a disk Read.   |
| 29,10 | P34,P35<br>HS0,HS1 | Head Select 0, 1 (HS0, HS1). Binary coded bits to select head 0, 1, 2, or 3.  |
| 40    | P36<br>WRTSM       | Write Sector Mark (WRTSM). (Output) Causes sector marks to be written on the disk if FMTEN is high and the Format jumper is installed.  |
| 4     | P37<br>RDHDR/TX    | Read Header/Transmit (RDHDR/TX). Command input to the Read/Write control circuits. If DRW (P27) is high and START/RSTERR (P26) is low, RHDHR hi will cause the leader field on the next sector to be stored in RAM. |

### Principles of Operation

Upon power up, the Z8 issues phase steps to the Head Stepper motor on the HDA to move the heads to track 77. The Z8 then performs a Read operation to read the Spares table. If this is successful, the firmware in the Z8 will perform the Scan sequence.

(For a more detailed explanation of what the firmware in the Z8 is doing (i.e., Scan, Seek, etc.), or information on the format used for the Pro-File HDA (i.e., Spares Table, sector header composition, etc.), refer to the Appendices section of this manual.)

The power up reading of the Spares Table and the performance of the Scan sequence are basically composed of Check Header and Read operations. These operations are discussed later.

Once the Scan is completed and the initial (operating system specific) handshake has taken place, the Pro-File remains idle until the Host requests an operation. All Host-requested operations in the Pro-File are performed in three steps: the Command Handshake, the Check Header function, and the Operation.

1. **The Command Handshake** - The Host sends command bytes to the Pro-File to tell it whether to perform a Read, Write, or Write/Verify operation, and on what logical block number to perform it.

The Z8 on the Controller PCB converts the logical block to location bytes (i.e., physical location on the disk; target head, track, and sector) and stores them in RAM.

The Command Handshake is the same for any of the three operations. (Read, Write, or Write/Verify).

(Continued on the following page.)

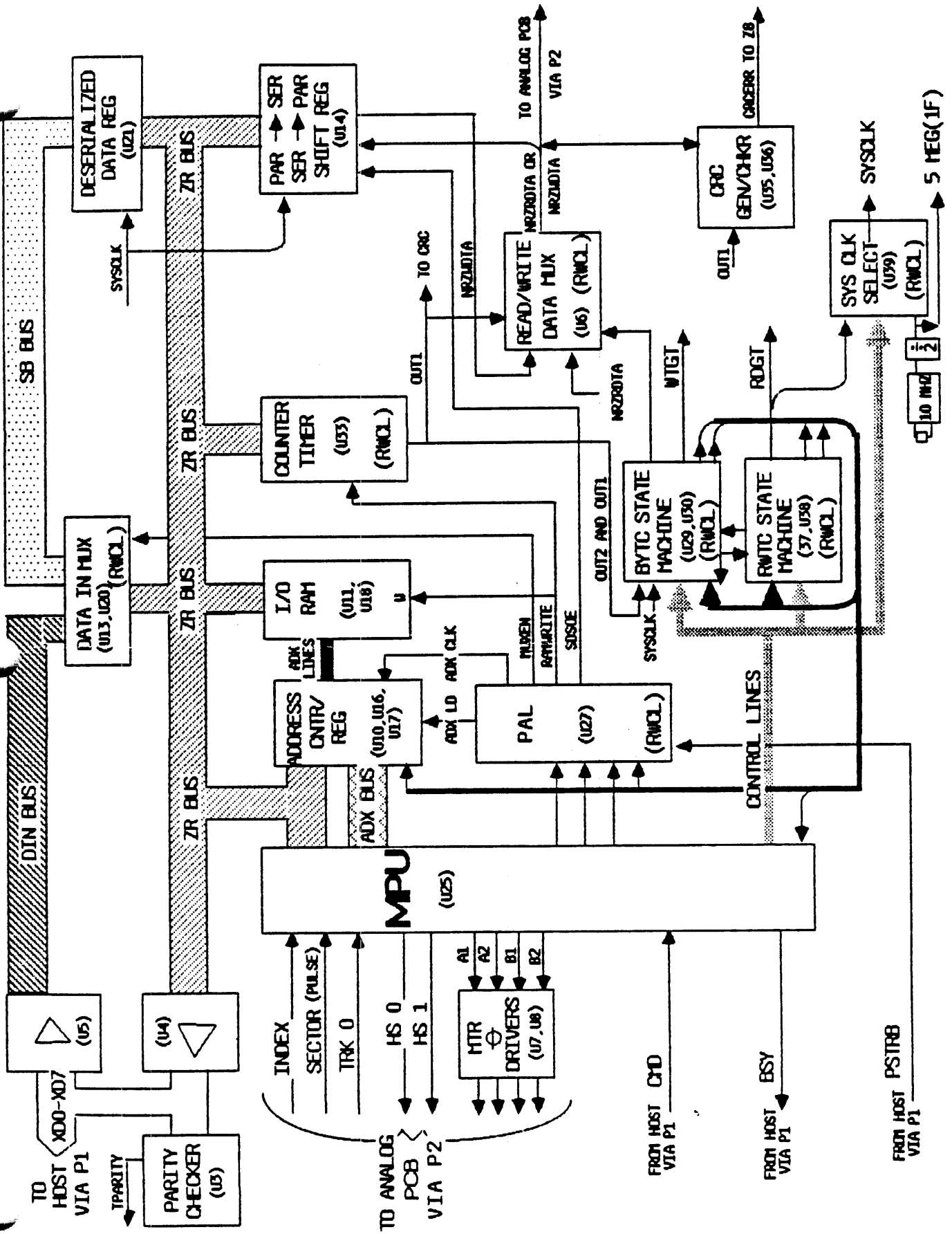
- 2. The Check Header Function** - If the target sector is on a different head or track from the one already selected, the 28 will perform the Seek routine to move all 4 heads to the target track (the track containing the target sector) and will enable the target head (the head over the disk surface containing the target track and sector).

The Seek routine then uses the Check Header function to read three consecutive sector headers from the track it has moved the head to, and compares them with the target head, track, and sector bytes in RAM.

The process used in the Check Header function to read the sector headers (to confirm a Seek to the right track) is almost identical to the first part of the Read, Write, and Write/Verify operations, which also read sector headers to find their target sectors.

- 3. The Operation** - Once a successful Seek is confirmed, the 28 coordinates the circuitry in the Controller PCB and Analog PCB to perform it. Each operation follows a different sequence of events.

CONTROLLER PCB BLOCK DIAGRAM



## Controller PCB Circuit Descriptions

### CONTROLLER PCB DETAILED BLOCK DIAGRAMS

The following is a brief description of each of the 17 functional elements on the Controller PCB. Understanding the functions of these elements will help you to understand the signal flow discussions later.

For more specific circuit diagram information refer to the Controller PCB schematic at the end of this section.

#### **Z8 Main Processing Unit U25**

The Controller PCB's MPU is a Z8 microprocessor, which has a self-contained ROM program. It provides an intelligent interface to the Host computer. It indirectly controls the Pro-File's electronics by setting modes and directly controls the stepper motor and head selection.

#### **PAL U27**

This single chip is a logic array specifically programmed for this application. It performs complex and/or combinational logic functions. Primarily, it controls the function of the address counter, the direction of data to/from RAM, loading the counter/timer, and the serial/deserial register.

#### **RAM Address Counter/Register U10, U16, U17**

The method of use depends on what operation is currently going on. This element can be preset to a certain point and counted up through a sequential range of addresses for RAM access. It is also used as an Address register where it is loaded with a value for a specific single access.

#### **RAM U11, U18**

The RAM is a two kilobyte RAM array used to hold data to and from the Host and disk. Various locations are used to hold status information and the current spares tables.

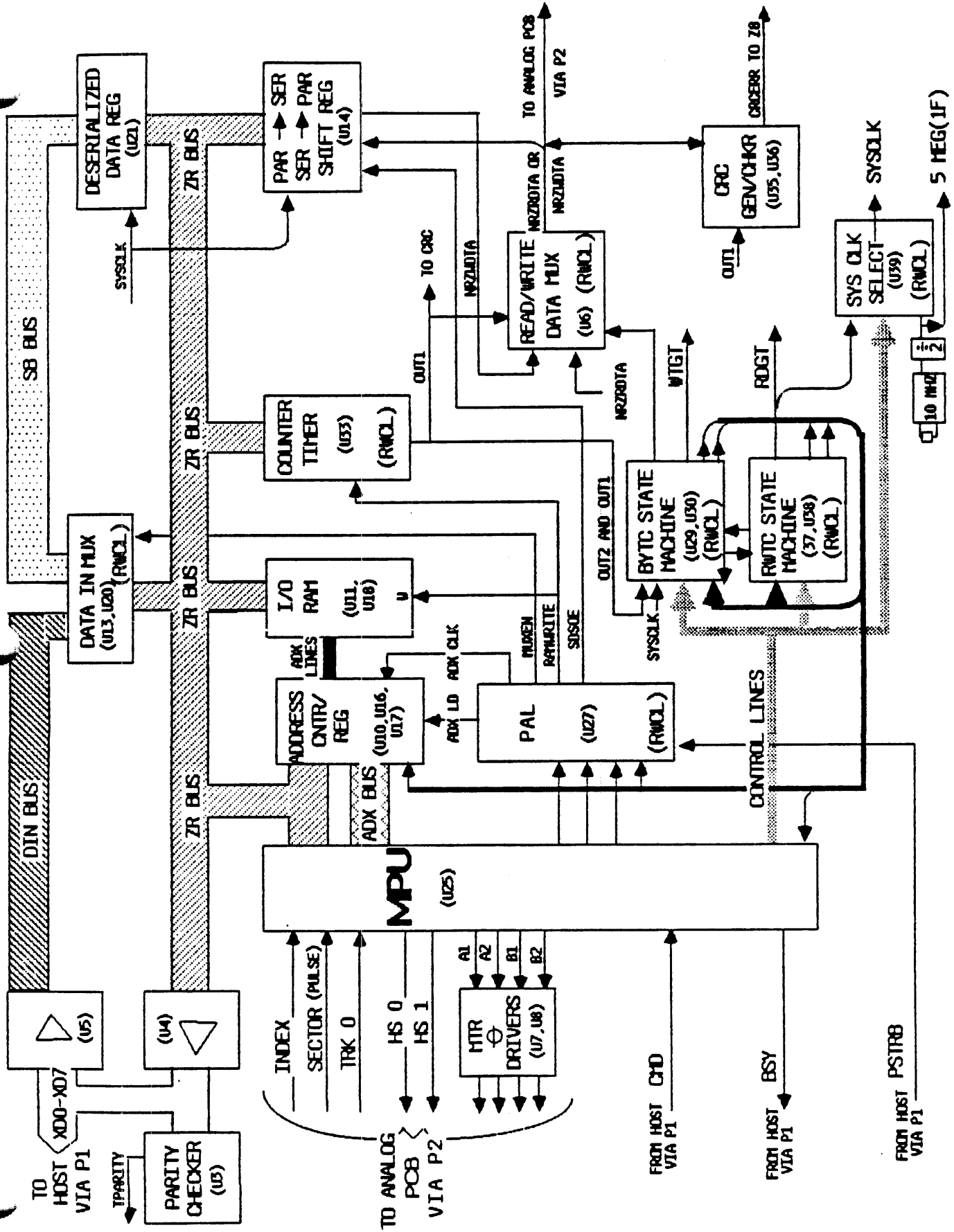
#### **Data Line Drivers U4, U5**

These simple Line Drivers drive data to and from the Controller and Host interface PCBs.

#### **Data In MUX U13, U20**

This MUX is used to direct data coming in from the Host interface PCB or from the disk. The usual destination of its outputs is the RAM.

CONTROLLER PCB BLOCK DIAGRAM



**Bus Parity Checker U3**

The BPC forms the other half of the bus parity checking circuit on the Host interface PCB. It constantly monitors the bus, checks the parity at the Controller end, and sends its sum to the Host interface to be compared with the sum on the interface end. A parity error should not occur unless a cable fault exists.

**BYTC State Machine U29, U30**

The BYTC (Byte Control) element of the State Machine, one of the two major elements of the Read/Write Control circuitry, steps through the control states for each part of an operation at a bit-time rate.

**RWTC State Machine U37, U38**

The RWTC (Read Write Timing Control) element of the State Machine, the second major element of the Read/Write Control, steps through the control states necessary to control the timing for all the operations associated with block/sector reading and writing.

**System Clock Selector U31, U32, U39**

The SSC switches from the crystal oscillator, used during idle and Write operations, to the Read clock generated by the Analog PCB during the Read operation. This keeps the logic in sync with the data.

**Divide-by-8 Counter**

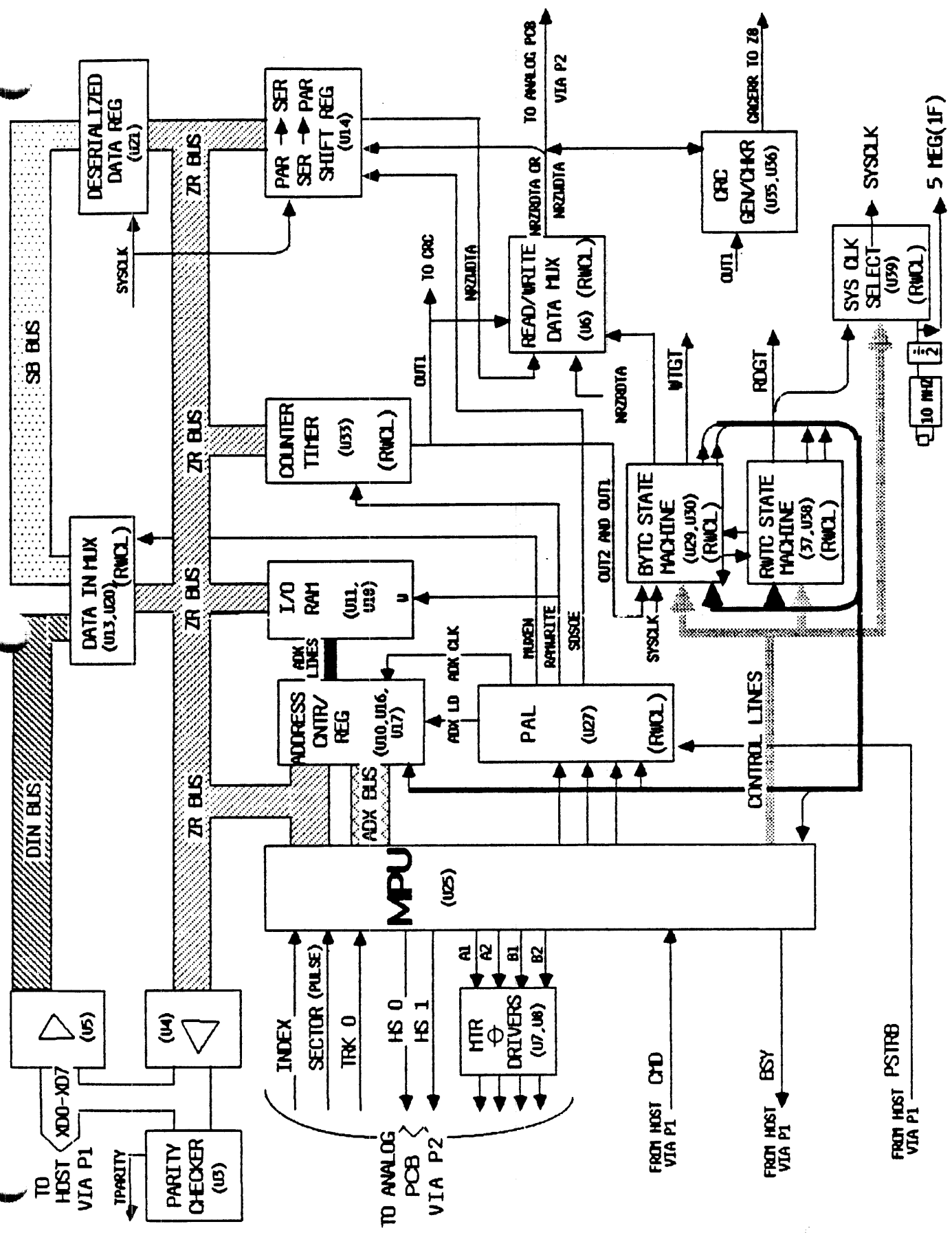
Counts the system bit-clocks that the System Clock Selector has selected (either the clocks from the Controller PCB's crystal oscillator or RDCLKs from the Analog PCB) and produces a positive transition from its QC output for every eight bit-clocks received (one per byte). Its QB and QA outputs enable the State Machine to discriminate phase (bit times) within the processing of a byte.

**Programmable Counter/Timer U33**

This chip receives the QC output of the Divide-by-8 Counter as its input clock. It contains three programmable counters, which yield byte-time information to the Read Write Control logic, and it basically keeps track of what part of the particular sector is being processed by the Controller PCB.



CONTROLLER PCB BLOCK DIAGRAM



## Controller PCB Circuit Descriptions

### **Read/Write Data MUX U6**

The Read Data MUX is used to select one of two sources of data, either Serialized Data from the SER/DESER register, or NRZ Read Data from the Analog PCB. When reading, it gates NRZ Read Data through to the Serial/Deserial Shift Register U14. During a Write, it gates serial data from the Serial/Deserial Shift Register U14, to the CRC generator U35.

### **CRC Generator/Checker U35, U36**

The CRC (Cyclic Redundancy Check) circuit is used to compute CRC check characters that are written at the end of each data block on disk during Write operations, to compute CRC for Read data, and to compare the result with the CRC characters that were read at the end of each data block

### **Deserialized Data Register U21**

This 8-bit register temporarily holds the deserialized data from the disk so that the shift register can receive the next byte. When the logic is ready, it directs the register's contents to RAM through the Data In MUX.

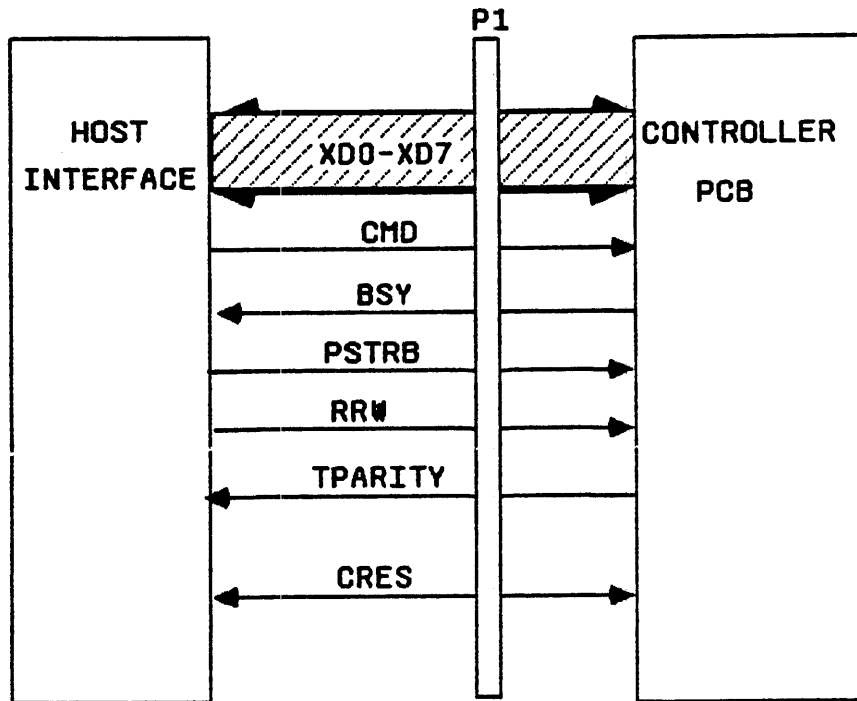
### **Serial/Deserial Shift Register U14**

This register is used to take the parallel data from RAM and shift it out serially to the Analog PCB and to take the serial data from disk and shift it into a parallel format for transfer back into RAM.

### **Stepper Motor Drivers U7, U8**

The 4 phases required for Stepper motor movement are generated by the Z8. The current for these signals is then boosted by the Stepper Motor Drivers U7, and U8.

## PRO-FILE HOST INTERFACE



## Controller PCB Circuit Descriptions

### CONTROLLER PCB SIGNAL FLOW DESCRIPTION

To understand Controller PCB operation, you should first become familiar with data flow in the three stages of an operation; the Command Handshake, the Check Header function, and the operation itself. The following discussions describe each stage, first in general and then in detail.

The Z8 is used to condition the logic, but it is not actively involved with data transfers to/from the disk or Host; that is done by the Read/Write Control logic (RWCL which is just about everything else on the Controller PCB except the Z8, RAM, and Host interface circuitry).

(For information on the Pro-File format on composition of the sectors in the format, refer to the Pro-File HDA Description in the Appendices section.)

#### A. Command Handshake

##### Command Handshake General Explanation

Assume that the Pro-File is initially sitting idle with the BSY line high (not active), the disks spinning, and the heads over track 155 (Park position), waiting for the Host to tell it to do something. The Host communicates this message during the Command Handshake.

The Host asserts CMD (active low) to initiate communications with the Z8. Upon seeing CMD going low, the Z8 lowers its BSY line and waits for the Host to raise CMD.

When the Pro-File sees CMD go high it places a 01 response byte on the interface bus and raises BSY.

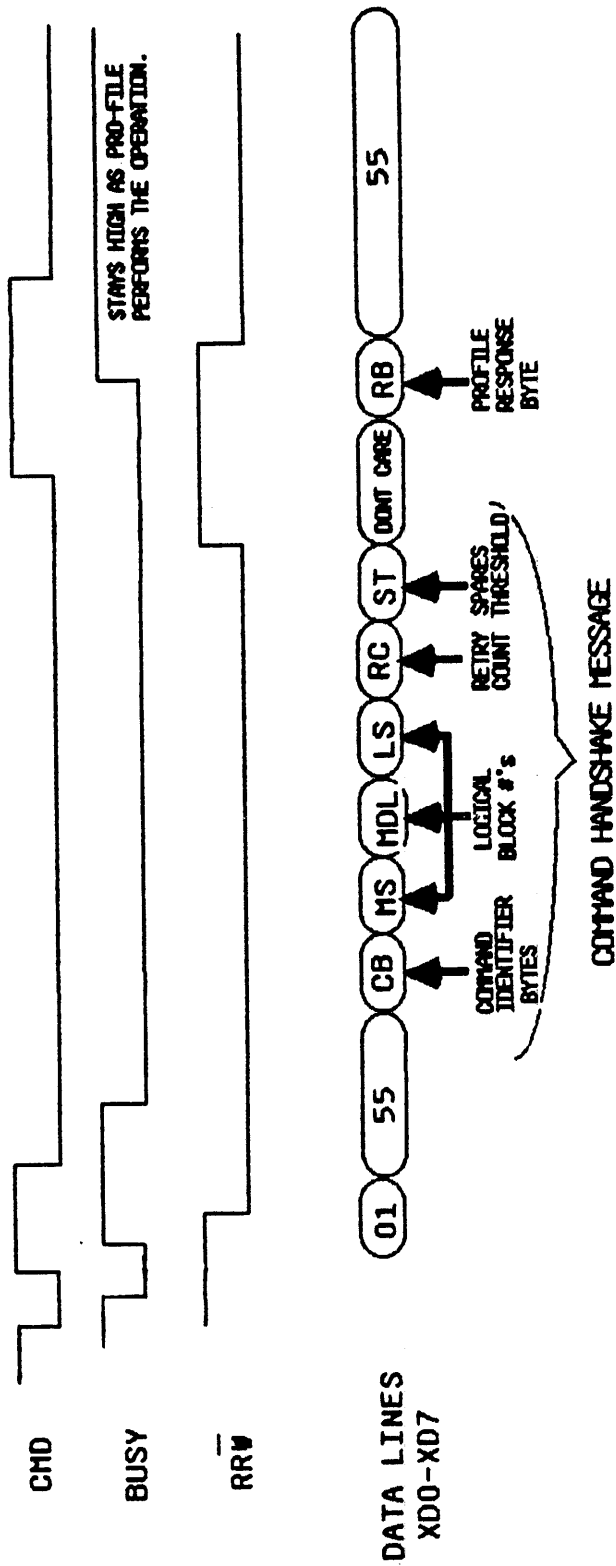
The Host sees the BSY line go high and interprets the 01 as an ACK, so it lowers the RRW signal. The low RRW signal enables the Pro-File to write the command bytes the Host will send into its RAM.

The Host must acknowledge the Pro-File's response with a 55, or the Z8 will abort the operation and go back to idle. The Host puts its 55 response byte on the bus and lowers the CMD line.

The low RRW and the response of 55 cause the Z8 to condition the bus to receive the command bytes, which are not immediately read by the Z8 but are stored in RAM for future reference.

After the Host puts each byte on the I/O bus, it generates PSTRB. The positive transition of the negative pulse PSTRB is used to clock the byte into the RAM.

# COMMAND HANDSHAKE TIMING



## Controller PCB Circuit Descriptions

When CMD goes low again, the Z8 interprets the command bytes and responds with the result of its command interpretation. For example, if the Host has said to read a block, the Z8 would respond with "02", which means "I'm going to read a block".

If it wants the operation to continue, the Host must confirm the response with a 55 on the bus again. If it disagrees or has changed its mind, the Host will send a byte other than a 55 causing the Pro-File to abort the operations.

Two handshakes are required to complete a Read operation. The first one is the Command Handshake, and the second is when the Pro-File sends the Read data, and the completion status of the operation back to the Host.

Three are required for both a Write and a Write/Verify operation. The first one is the Command Handshake, and the second is when the Host sends the block of write data to the Pro-File, and the third is when the Pro-File sends the completion status of the operation back to the Host.

The command identifier bytes for each of the three commands are as follows, 00 for Read, 01 for Write, and 02 for Write/Verify. A Command Handshake message is composed of the following elements.

<u>Command Identifier</u>	<u>Logical Block #</u>	<u>Retry Count</u>	<u>Sparing Threshold</u>
XX	Most, Middle, and Least Significant	Host Specific	Host Specific

The Pro-File interprets CMD high as a request from the Host to send a byte telling the Host what the Pro-File expects to do next. When the Pro-File is waiting for a command, it sends an '01' in response to CMD high. The Pro-File's other responses are shown in the table below.

<u>Host's command to Pro-File</u>	<u>Pro-File's Response</u>
Initiate handshake (lowers CMD)	01
Read a block	02
Receive Write data	03
Receive Write/Verify data	04
Do the Write or W/V on disk	06

## Controller PCB Circuit Descriptions

Following a Read or a Write, the Z8 provides the Host with four status bytes, which are placed in the buffer immediately preceding the data just read or written. The significance of the individual bits is listed below:

### STATUS 1

- 7 = 1 if Pro-File received 55 to its last response
- 6 = 1 if Write or Write/Verify was aborted because the number of data bytes sent exceeded the data block limits or because the Pro-File couldn't read its spares table
- 5 = 1 if the Host's data is no longer in RAM because the Pro-File updated its spares table.
- 4 = 1 if SEEK ERROR - caused by Pro-File being unable in three tries to read three consecutive headers on a track
- 3 = 1 if CRC error, may occur only during an actual Read or verify of Write/Verify, not while trying to read headers after seeking
- 2 = 1 if TIMEOUT ERROR (couldn't find target sector's header in nine revolutions - Not set while trying to read headers after seeking)
- 1 = N.C.
- 0 = 1 if operation is unsuccessful

### STATUS 2

- 7 = 1 if SEEK ERROR - occurs if Pro-File is unable in one try to read three consecutive headers on a track.
- 6 = 1 if spares table overflow (More 32 sectors spared)
- 5 = N.C.
- 4 = 1 if bad block table overflow occurs (Less than 100 bad blocks in table )
- 3 = 1 if the Pro-File is unable to read its status sector.
- 2 = 1 if sparing occurs.
- 1 = 1 if Seek to wrong track occurs.
- 0 = Not used.

## Controller PCB Circuit Descriptions

### STATUS 3

- 7 = 1 if the Pro-File has been reset
- 6 = 1 if block number is invalid
- \* 5 = 1 if block I.D. at end of sector is mismatched
- 4 = N.C.
- 3 = N.C.
- \* 2 = 1 if the Pro-File has been reset.
- \* 1 = 1 if the Pro-File gave a bad response
- \* 0 = 1 if CRC error occurs.
- \* These bits are sent by the Host driver.

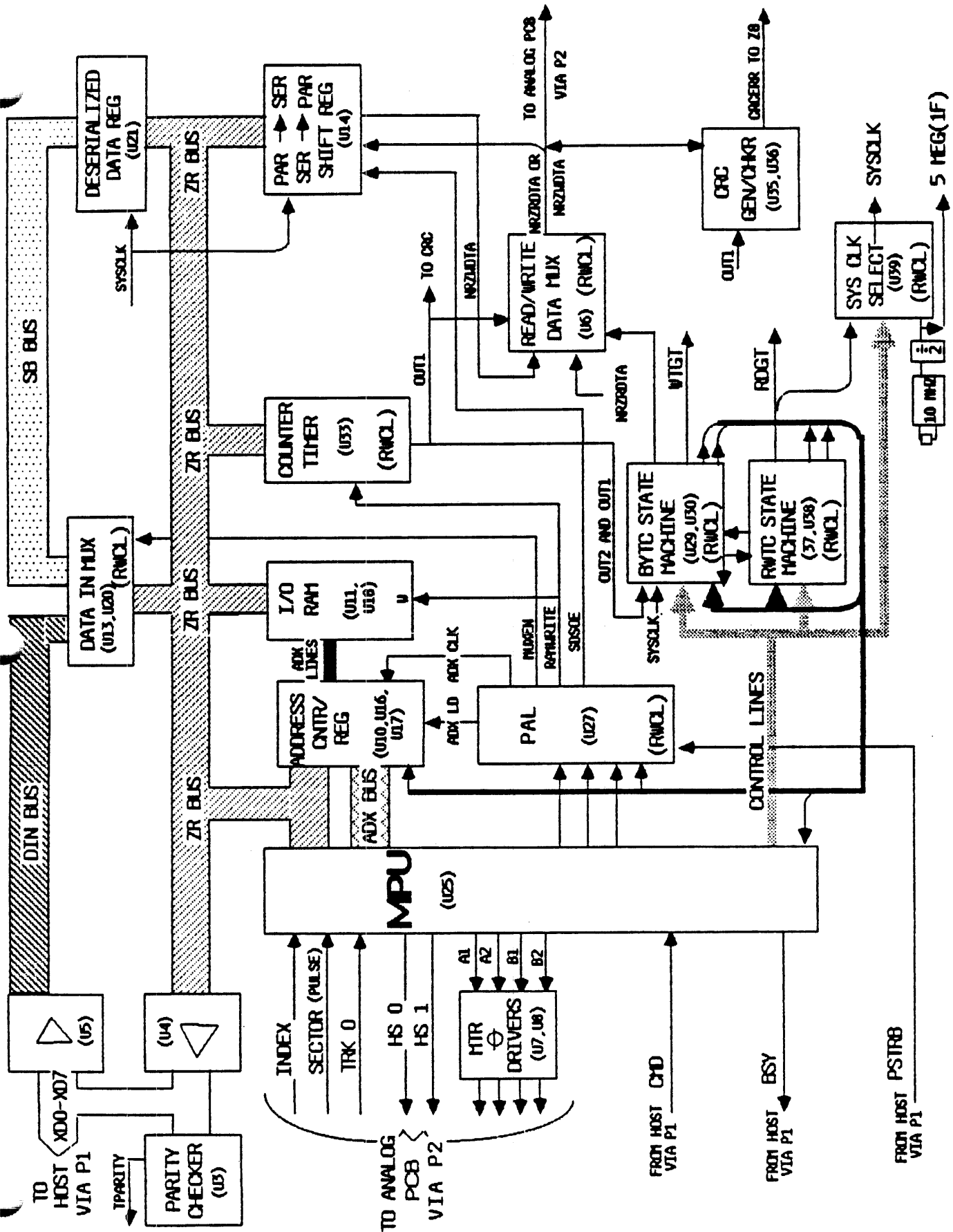
### STATUS 4

- 7 - 0 = the number of errors encountered when rereading a block after any read error.

(Continued on the next page.)



CONTROLLER PCB BLOCK DIAGRAM



## Controller PCB Circuit Descriptions

When the Host interface's CMD signal goes high, the Z8 responds by sending a "01" response byte up to the ZR bus, and off to the left through the buffer to the Host interface. (See figure on the opposite page).

The Host lowers RRW and CMD. When the Host interface lowers CMD, the Z8 should see the Host's "55" acknowledgement coming in through the buffer to the Data In MUX directly to the Z8. This acknowledgement and RRW's being low triggers the Z8 to get the RAM ready to accept the command bytes.

After the first handshake of CMD and BSY, the Host transfers the actual command and delimiting bytes. They come, as do all data, from the Host through the Data In MUX, and are then stored in RAM.

The Z8 then evaluates the command bytes by bringing them in from RAM. After interpreting the command bytes, the Z8 gives its response byte, which is ack'd or nack'd by the Host.

## Controller PCB Circuit Descriptions

Refer to the Controller PCB schematic at the end of this section for the following discussion.

### Command Handshake Component Explanation

1. When the Host lowers CMD to pin 33 of the Z8, the program in the Z8 will lower BSY on pin 34. When the Host raises CMD, the Z8 puts a 01 on the bus and signals the Host by raising BSY.

Because RRW is already high to pin 4 of U9, the direction of the data on the bus is from the Pro-File to the Host.

2. The Host interprets the 01 as an ACK and lowers RRW, which changes direction of the bus. Then it places 55 on the bus and signals the Pro-File by lowering CMD.
3. The first phase of every operation is always the same, so the program in the Z8 knows that after sending the 01, the Host should respond with a 55. The Z8 must enable the contents of the DI bus (should be a 55) to be gated onto the ZR bus so that it can verify that the Host has sent a 55.
4. To do this, the Z8 generates the low MSEL1 and MSEL0 signals, to enable the Write Multiplexers (U12 and U20) to select the inputs from the DI bus.

Once the Z8 senses that CMD has gone low (an indication from the Host that it has put the data, in this case 55, on the data lines), it sends to PAL (U27) the combination of inputs it needs to generate the MUXEN signal, which gates the DI data onto the ZR bus.

(For a table showing the conditions necessary to generate PAL signals, refer to the PAL Function Table at the end of this section.)

5. With the signals described above, a data path is established to pass the 55 from the DI (Data In) bus, through the Data In Multiplexers (U13, and U20), and onto the ZR bus. The Z8 then reads the 55 from the ZR bus.

6. The Z8 now knows that it will receive some command bytes telling it what operation the Host is requesting, so it puts the first address it wants the command bytes stored in on the ZR bus and causes the PAL to generate the LD (Load) pulse to pin 9 and the clock to pin 2 of each Address Counter.

This presets the Address Counters to the address in which it wants to store the first command byte. **Note:** A10 in the address must be low to select RAM.

7. The Data In Multiplexers (U12 and U20) are still enabled to select the DI bus inputs and pass them to the ZR bus.

(Recall that after the Z8 read the 55 (Step #3), it sent to PAL (U27) the combination of inputs it needed to generate the SEL signal to RAM).

8. A data path is now established to pass the command bytes that will shortly follow from the Host to the DI (Data In) bus, through the Write Multiplexers (U13 and U20), onto the ZR bus.

9. The Host waits a short period after each byte is put on the lines for the data to settle, and then generates the PSTRB signal.

10. Because of the PAL's current inputs, the PSTRB signal causes the PAL to generate the RAMWRITE signal from pin 16, which stores what is on the ZR bus into the RAM address specified by the Address Counters.

11. PSTRB also causes the PAL to generate an Address Counter Clock from pin 19, to increment the Address Counters for the next byte to come in.

12. When the Host has finished sending bytes, it raises RRW to pin 4 of U9, to change the direction of the Data bus.

The Host then raises CMD again to tell the Z8 that no more command bytes are coming. Now the Z8 reads the command bytes from RAM to interpret them.

## Controller PCB Circuit Descriptions

13. To read the command bytes, the Z8 sequentially sets the Address Counters to the addresses of the command bytes.

RAMSEL and an address on the lines to the 2114-type RAM fully enable the RAM to put the contents of the address on the ZR bus. As each command byte is read onto the ZR bus, the Z8 reads and interprets it.

14. If the command is for a Read, the Z8 will respond by putting 02 on the ZR bus.

If the command is for a Write, the response byte will be 03. If a Write/Verify, the response byte will be 04.

After the Z8 puts the response byte on the ZR bus to the Host, it asserts BSY, signifying it is now performing the operation. The response byte is driven by U4 to the interface of the Host.

15. The Host checks the response. Because it knows which command it requested, it knows which response byte to expect.

Since the response byte is 02, as expected, the Host acknowledges with 55 and raises CMD (it is true when low, so high means CMD is deactivated).

16. The Command Handshake is now complete. Once the Host raises CMD, the Z8 performs (if necessary) a Seek routine (explained later) to select the proper head and move it over the target track.

17. If the command is a Write or Write/Verify, then there will be another handshake to transfer the Write data during the Seek routine.

18. If the command is a Read, then once the proper head is selected and positioned over the target track, and the Seek has been verified, the Z8 will perform the Read.

## B. Check Header Function

### Check Header Function General Operation

For each Read or Write operation, the specific sector must be located and checked. This is accomplished by the the Z8, and the Read/Write Control Logic, during the Check Header function.

Before the Z8 conditions the logic to start a Read, Write, or Write/Verify operation, it translates the logical block number requested by the Host into target sector information bytes (i.e., head, track, and sector). It then checks to see if the desired block is in the spares table and sets the track, head, and sector accordingly.

The Z8 then sets a complete replica of the target header into a specific area of RAM. (For more information on the Seek routine and other firmware routines used in the Pro-File Z8, refer to the Firmware Routines Description.)

### Seek Routine

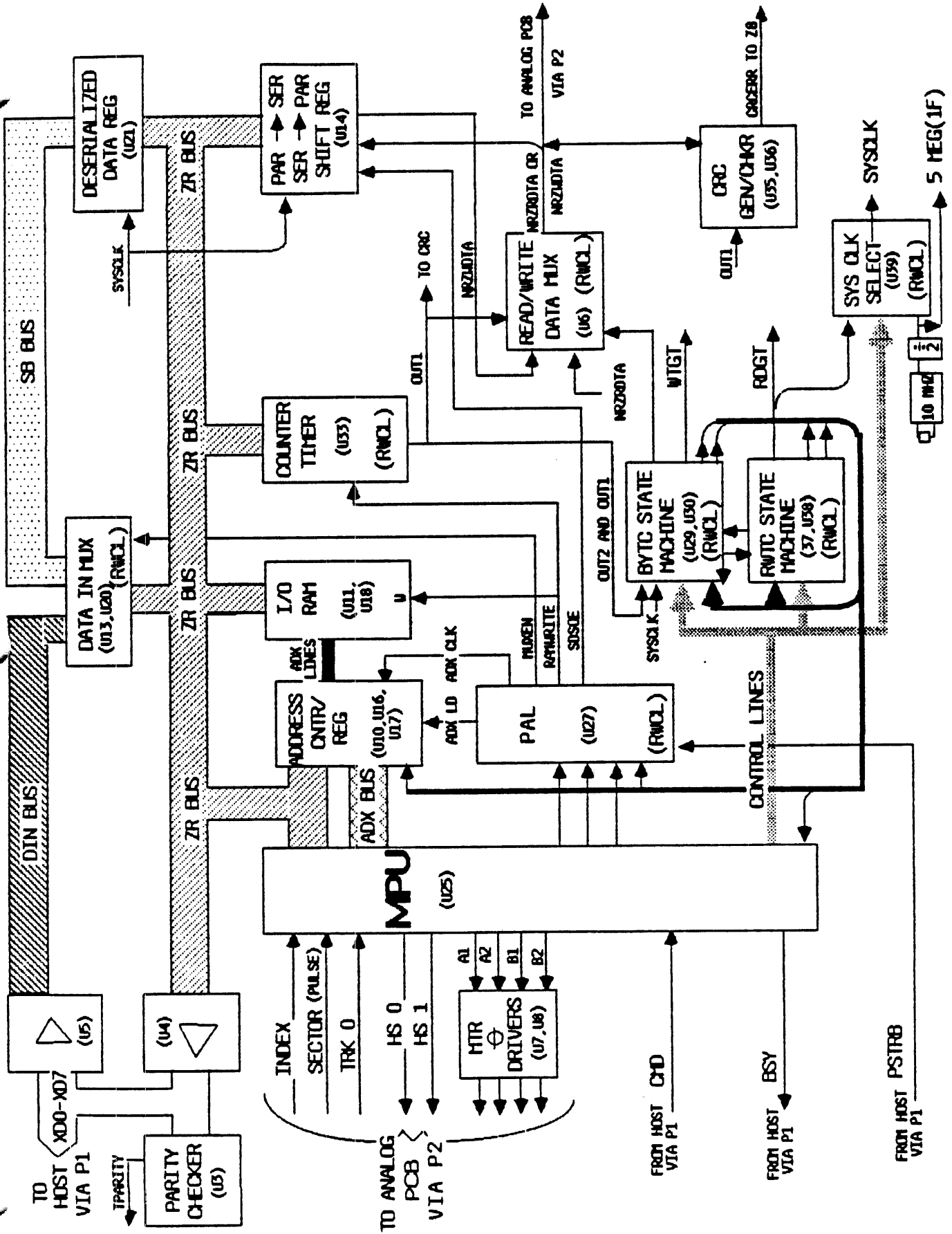
The Seek routine is a firmware routine in the Z8. It controls selecting the proper head, positioning the heads, and putting the Read/Write Control Logic in the proper modes for a Check Header function after it has moved the selects

If the current block and the last block read or written have the same track and head, the Z8 will exit the Seek routine because the target head is assumed to be positioned over the target track.

If the track is the same but the head is different, the Z8 will send out enable signals to the target head, wait 750us, and then exit the Seek routine to perform the Host-requested operation.

If the track is different, the Z8 will generate the proper number of stepper pulses on the stepper phase control lines to position the head where it thinks the target track should be. Then it waits for the sector pulse, generated by the Analog PCB when it detects a sector mark.

CONTROLLER PCB BLOCK DIAGRAM



## Controller PCB Circuit Descriptions

When the Z8 sees the sector pulse it starts the State Machine.

(For more information on sector headers and Pro-File disk format refer to the Pro-File HDA description in this section.)

### Block Diagram For Check Header Operation

The State Machine, in combination with the PAL, moves each successive byte of the header replica into the SERIALIZER, where they are serialized and shifted out in sync with the incoming NRZDTA.

The target header information and the NRZDTA are compared, and if any difference exists, the State Machine aborts the attempt and resets to wait for the next incoming sector pulse.

The process is repeated until either the header matches the image in RAM or a timeout error occurs (the Z8 program is waiting for the "sector done" from the State Machine). If it doesn't see SECTDN within two revolutions, the Z8 will take over and go through an error recovery routine.)

If the desired operation is to read a block, the logic will accept the data in from disk and will move it into RAM. If the operation is to write a block, the logic will be conditioned to move the data from RAM to the disk.

The circuit description for Check Header function and the Read, Write, and Write/Verify operations are described in the following pages.



Refer to the Controller PCB schematic at the end of this section for the following discussion.

**Check Header Function Component Explanation**

1. After the Command Handshake, if the Z8 firmware has interpreted the command, the first thing it will do is put the location of the target sector (i.e., head, track, and sector) in RAM. The Z8 selects the RAM addresses the same way it did when reading the command bytes in the Command Handshake (with the Address Selectors).
2. If the target sector is on a different head or track than the ones already selected, the Z8 will perform the Seek routine to the target track (the one containing the target sector).

During the Seek routine, the Z8 issues phases from pins 17-20 through U7 and U8 to the Head Stepper motor on the HDA. It issues the exact number necessary to put the heads where it thinks the target track is (this is a program function of the Z8).

3. When the head movement is completed, the Z8 enables (loads) the target head.
4. At this time, the Z8 lowers ZRW and AS to cause the PAL to produce the TIMSEL signal out of pin 12 to the Programmable Counter Timer U33. The Z8 then writes commands to the Programmable Counter Timer U33 to program the following registers:
  - a. OUT1 register for 555.
  - b. OUT2 register for 557.
  - c. OUT3 register for 521.

The counts are shown in the diagram on the opposite page with the events they are timing.

(Continued on the next page.)

## Controller PCB Circuit Descriptions

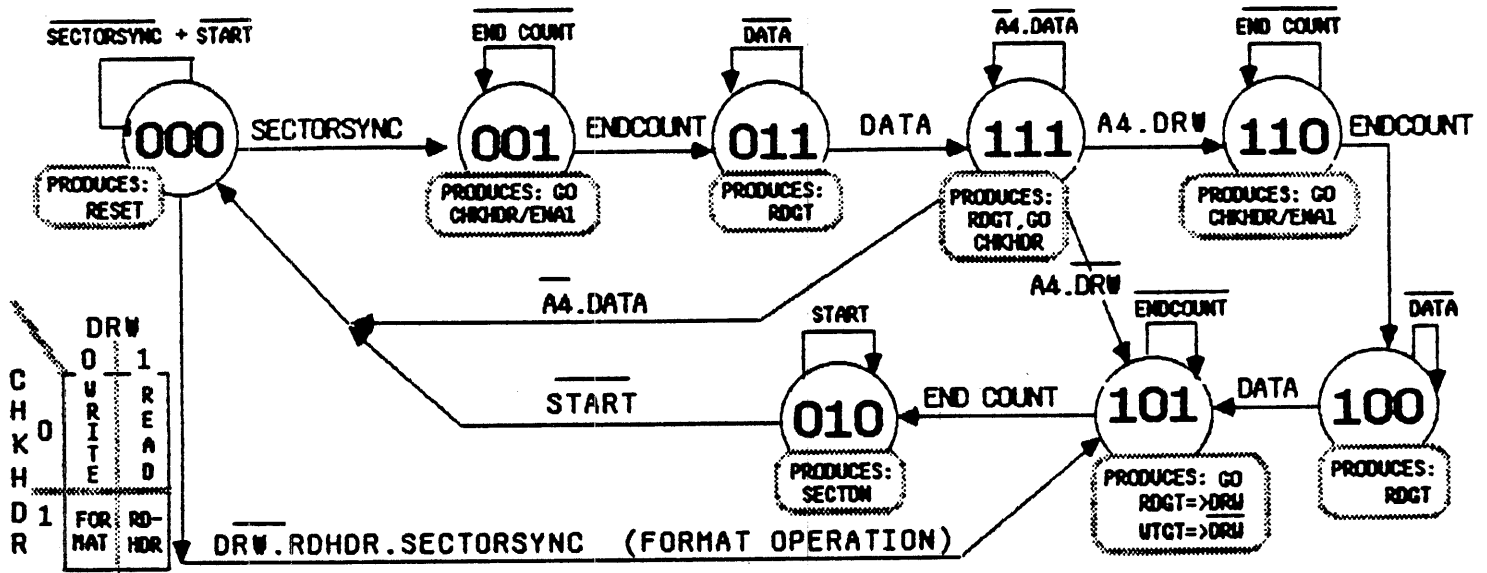
5. The Z8 then causes the SEL signal out of pin 17 of the PAL to be generated. This enables the RAM to gate the contents of address 0 (since that is the address in the Address Counters at this time) onto the ZR bus to the inputs of U14, the Deserializer Shift register.

**Note:** Addresses 0, and 1 both contain all 0's. The sector location information begins with the track at address 2.

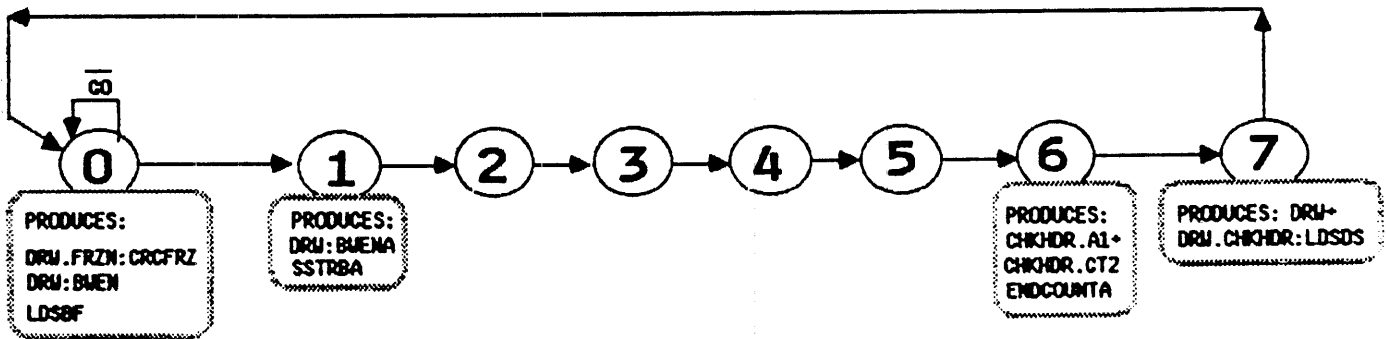
6. The Z8 then generates the START signal to:
  - a. Remove the reset to enable the CRC Error FF.
  - b. Remove the reset to enable the storage FFs for the Programmable Counter/Timer in U34.
  - c. Remove the reset to enable pin 13 of U39 the System Clock Selector.
  - d. Remove the reset to enable the latches in the BYTC (U30) and RWTC (U38) State Machine.
7. When the Analog PCB detects a sector mark (gap) on the target track, it generates the SECTOR signal to pin 30 of the Z8 and pin 15 of U30, the latch for the BYTC State Machine, causing the State Machine to advance from sequence 0 to sequence 1.

(Continued on the next page.)

## STATE MACHINE SEQUENCE DIAGRAM



## STATE MACHINE PHASE (BIT TIME) DIAGRAM



### State Machine Operation

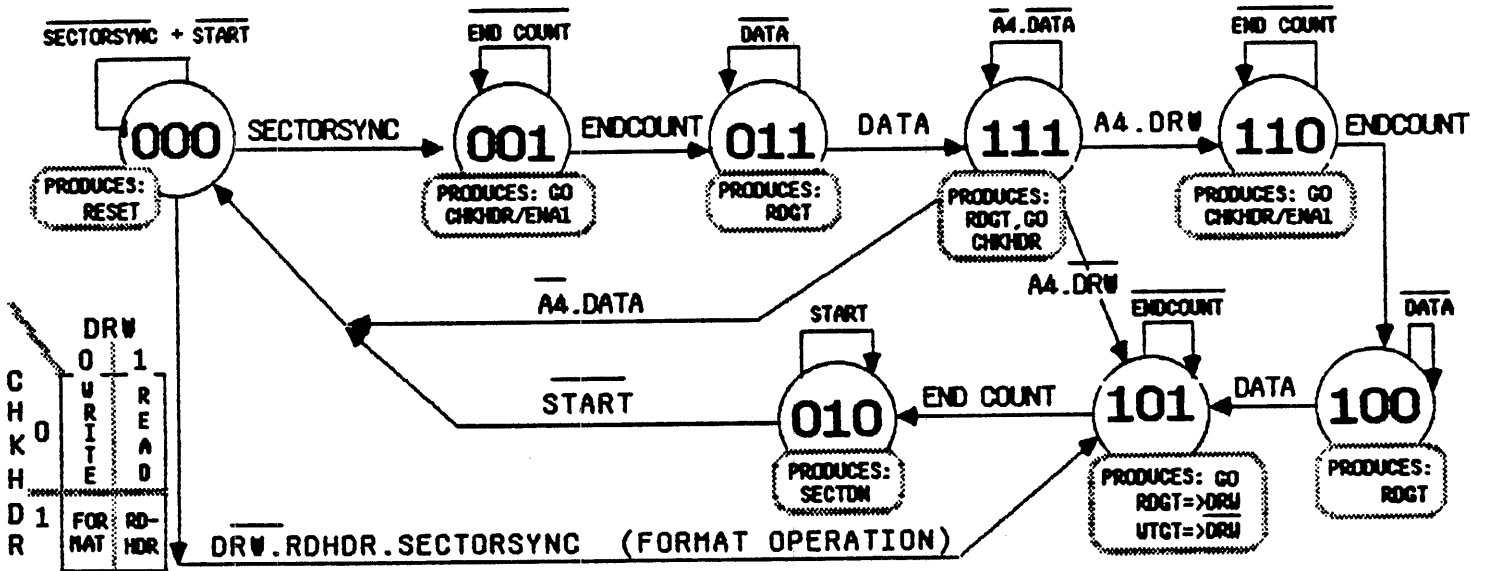
8. Each State Machine is composed of a ROM device and a latch. The inputs to the ROM select the ROM address to be read out. The bits in the contents of this address are used as control signals or select inputs to the latch. The outputs of the latch feed back around to the inputs of the ROM to select the next address in the sequence.
9. Various events (i.e., SECTOR, ENDCOUNT, DATA, etc.) determine the sequence of the ROM addresses to be read out and, therefore, which control signals will be enabled. These control signals regulate the sequence of functions that must occur for each operation. The sequences for the Check Header function are discussed under that header.
10. Refer to the diagram at the top of the opposite page for the following discussion. It shows the sequence of State Machine paths and the conditions that determine the next path to be selected. For example, the diagram shows that during sequence 0, the critical signal that the Controller PCB is waiting for is SECTORSYNC (sector mark).
11. Once that signal occurs, depending on whether RDHDR is true or not (RDHDR is only true while formatting the HDA), a path is selected to sequence 1 or 5. During normal operation, RDHDR is low, so the State Machine advances to sequence 1.

At sequence 1 the critical signal is ENDCOUNT. When ENDCOUNT occurs in sequence 1, the only path is to sequence 3, etc.

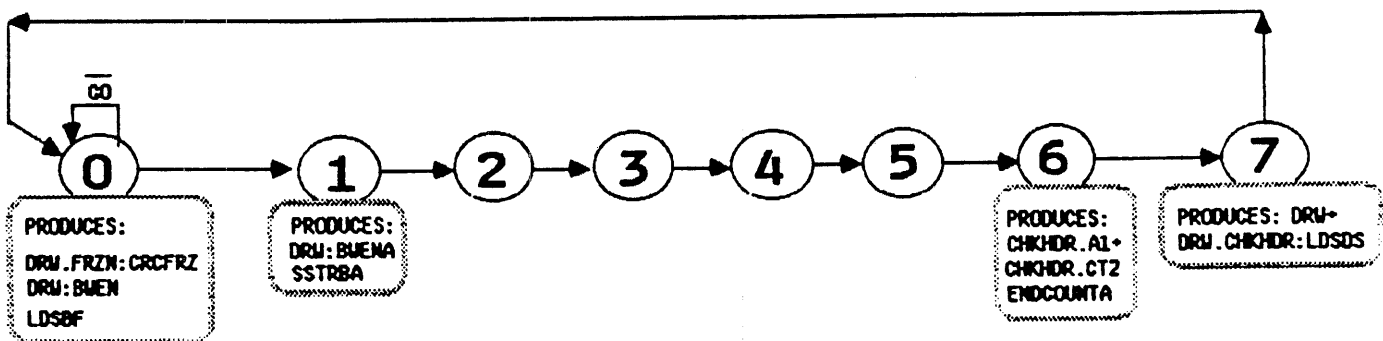
This diagram is true for all operations. During the Command Handshake, the Z8 interprets the command bytes from the Host to determine the operation requested.

(Continued on the next page.)

## STATE MACHINE SEQUENCE DIAGRAM



## STATE MACHINE PHASE (BIT TIME) DIAGRAM



## Controller PCB Circuit Descriptions

12. As an operation is implemented, the Z8 and PAL control the selection of sequence paths with their inputs to the State Machine (i.e., A4, RDHDR, CHKHDR/ENAL, DRW).
13. The program in the Z8 selects these signals depending on which operation it is trying to implement.
14. The State Machine Phase diagram at the lower part of the opposite page shows when (at which bit time in the processing of a serial byte) a signal may occur during a sequence.

For example, during sequence 7, every time a complete byte of data has been processed (QC goes high, indicating 8 clocks have been counted by the Divide-by-8 Counter U22) at clock 1 of the next byte, an SSTRB signal is generated out of pin 15 of U38.

Although neither of the diagrams shows the sequence during which SSTRB will occur, the lower diagram does show the bit time of a byte when it might become active.

(Continued on the next page.)



15. Sequence 0 is a wait state for the State Machine. When the SECTOR signal occurs to pin 13 of U30, it produces a low to pin 19 of U37, selecting the ROM address that advances the RWTC State Machine to sequence 1.
16. During sequence 1, the GO signal is generated out of pin 14 of U37 (see Timing Diagram). The GO signal enables the Divide-by-8 Counter to count clocks. During sequence 1 the clocks selected by the System Clock Selector U39 are those generated by the crystal oscillator.
17. To review what has happened so far: We are still in the Check Header function. The heads have finished their movement, and the proper head has been enabled. Now the Z8 wants to confirm that the target head is in fact over the target track, which it does by reading three consecutive sector headers and comparing their header information with target head and track information currently in RAM.

After the initial setup, the Controller PCB waited for the Analog PCB to detect a sector mark that signified that the beginning of a new sector was about to pass under the selected head. When the SECTOR pulse occurred, it advanced the State Machine to sequence 1.

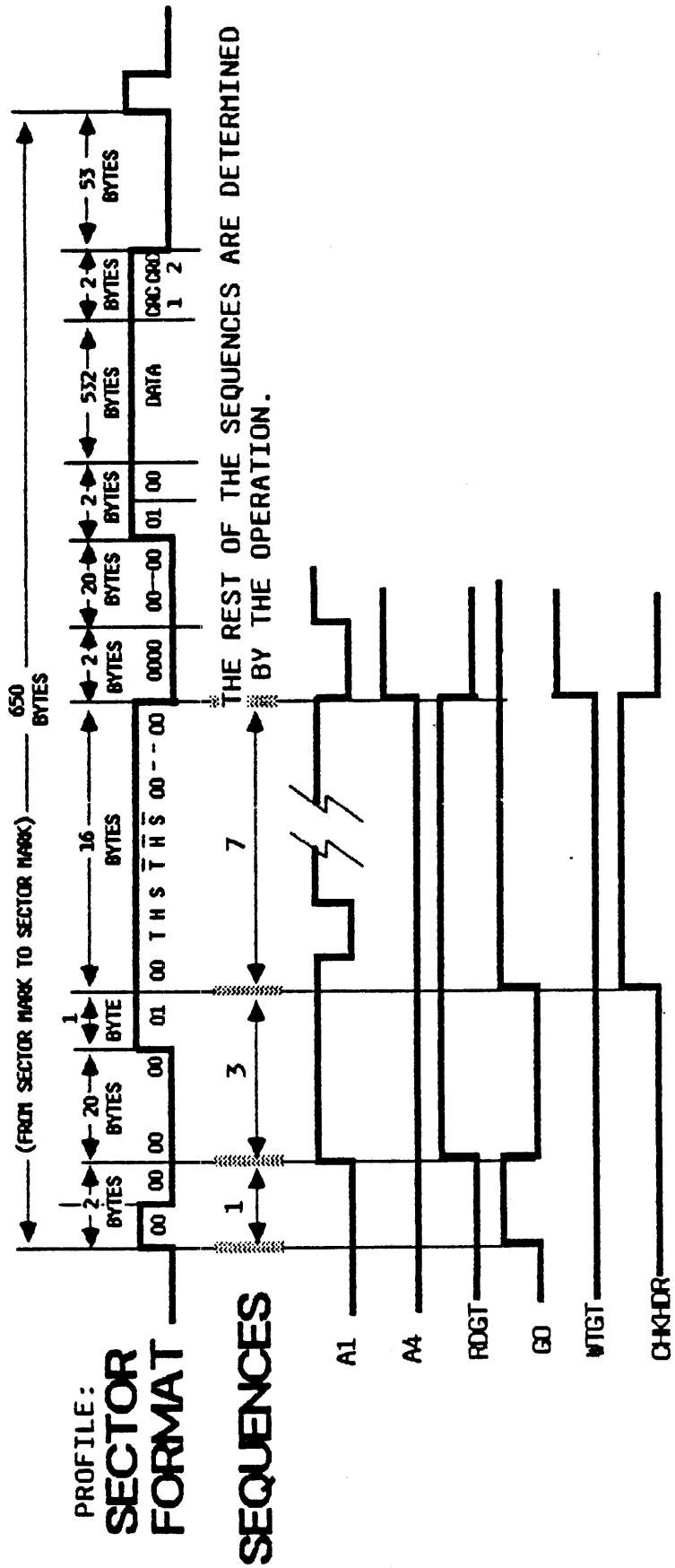
The sector header is the first part of the sector after the first sync byte field. The Z8 doesn't want to read the first two bytes of any sync byte field because they are unreliable.

So sequence 1 is simply a control state to hold the circuitry for the first two sync bytes, in case spurious data occur during that period. (For more information on the composition of a sector, refer to the Format description of the Pro-File HDA Description in the Appendices section.)

18. Every time the Divide by 8 counter counts 8 bit-clocks it produces a positive transition on its QC output. This signal goes to the clock input of the Programmable Timer (U33), which decrements each of its counters once for every pulse.



# CHECKHEADER SEQUENCE TIMING



## Controller PCB Circuit Descriptions

19. Each QC also goes to the State Machine, causing U38 to produce the SSTRB pulse out of pin 15 at phase 1 of the following byte. This signal goes to the PAL on pin 7, causing it to increment to the next Address.
20. The SSTRBs from the first two sync bytes cause the Address Counters U10, 16, and 17 to increment to a count of 1 (from 0). This causes the signal A1 to go to pin 5 of U29, causing the State Machine to produce the ENDCOUNT signal putting the State Machine in sequence 3.
21. Sequence 3 allows time for the VCO on the Analog PCB to sync to the sync byte field. While this is happening the Controller PCB is waiting for data (in this case the sector header). In sequence 3, the RDGT signal (pin 7 of U38) is generated by the State Machine.

This signal goes to the Analog PCB to enable it to convert the analog signal from the HDA head into NRZ data (NRZRDTA) and to generate RDCLKs in sync with this data.

RDGTA also goes to the System Clock Selector U31 and U32 to select RDCLKs as the system bit clock.

22. Sequence 3 also causes the GO signal to go low from pin 14 of U37 in the State Machine. The low GO signal resets the Deserializer chip (U14). This condition causes a low output from pin 17 of U14, which goes to pin 13 of the Exclusive Or in U28.
23. Pin 12 of U28 is NRZRDTA. At this point in reading the sector, NRZRDTA should be all 0's (because the sync bytes are all 0's), so pin 12 should be low, which, along with the low pin 17, results in a low out of pin 11 of U28.
24. Pin 11 remains low until the sync byte just before the sector header (which contains a 1) occurs; now the inputs to the Exclusive Or are different, making DATA signal on pin 11 high.



## Controller PCB Circuit Descriptions

25. As can be seen from the State Machine Sequence diagram, the high DATA signal is the condition that causes the State Machine to advance to sequence 7.

The purpose of sequence 7 is to read the sector header field of a sector. Recall that the Address Counters are pointing to RAM address 01, which contains 0's. The Z8 has the first byte of the target sector header field waiting on the ZR bus (this byte is always a 00).

26. When the State Machine advances to sequence 7:

- a. The LDSDS out of pin 12 of U29 goes high, causing the Deserializer to load the 00 from RAM address 1 (the first byte in the sector header should also contain a 00).
- b. Every QC output from the Divide-by-8 Counter (happens once per byte) to pin 3 of U29 will cause pin 8 to go high, causing the SSTRB signal out of pin 15 of U38.
- c. The CHKHDR signal out of pin 10 of U38 goes high, enabling the PAL to pass SSTRBs through as Address Counter increment pulses to the Address Counters.

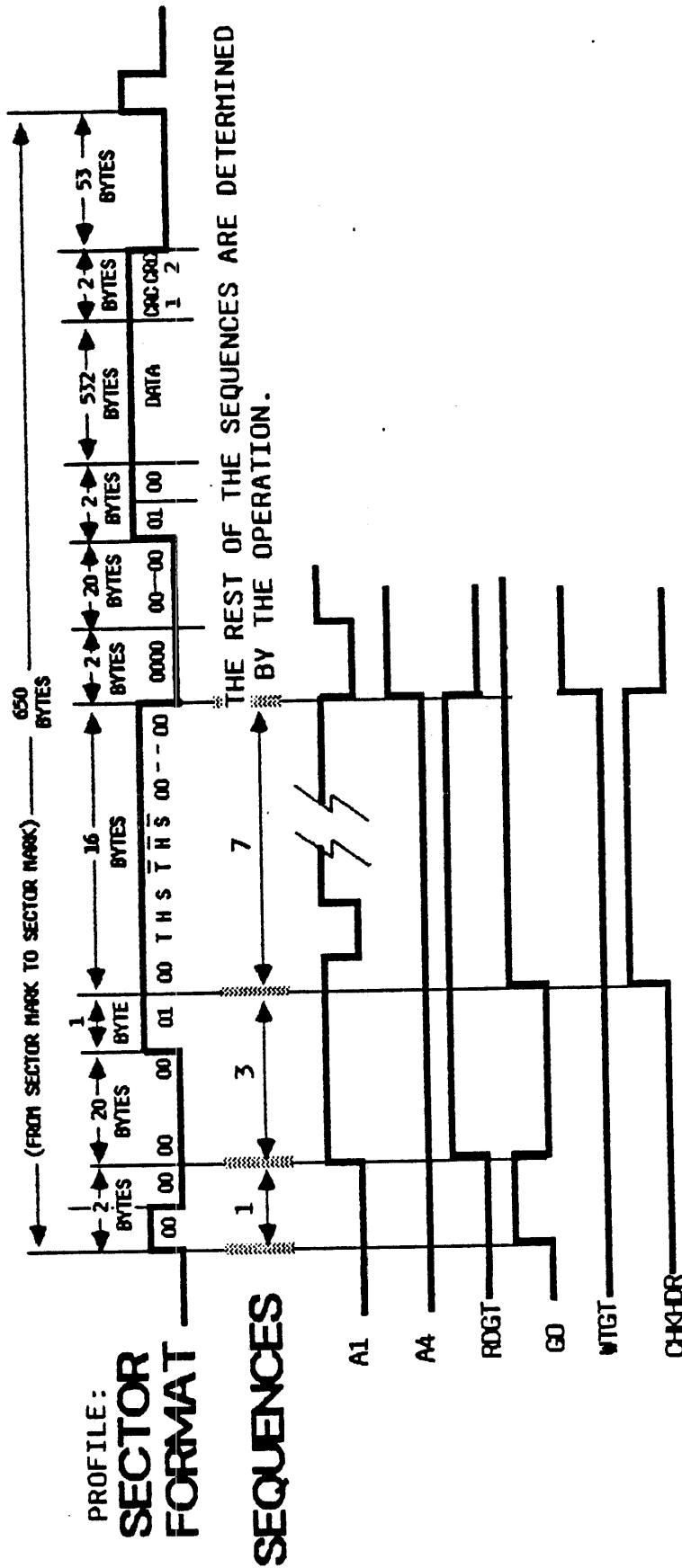
27. NRZRDTA that comes in during sequence 7 should be sector header information. The first byte of target sector header information in the Deserializer is clocked out in sync with the NRZRDTA coming in from the Analog PCB.

These two signals are compared in the Exclusive Or in U28. If any bit does not match up, this gate will output high causing the State Machine to generate a SECTDN signal out of pin 2 of U30, resetting the Read/Write Control circuitry to sequence 0.

28. If the first byte is correct, the QC output from the Divide by 8 chip U22 will cause an SSTRB to increment the Address Counters at bit 1 of the next byte.

This signal puts the next byte of target sector location information on the ZR bus. At bit 7 of that byte, if the comparison is still OK, LDSDS will occur to load the second byte of target sector location information into the Deserializer chip.

# CHECKHEADER SEQUENCE TIMING



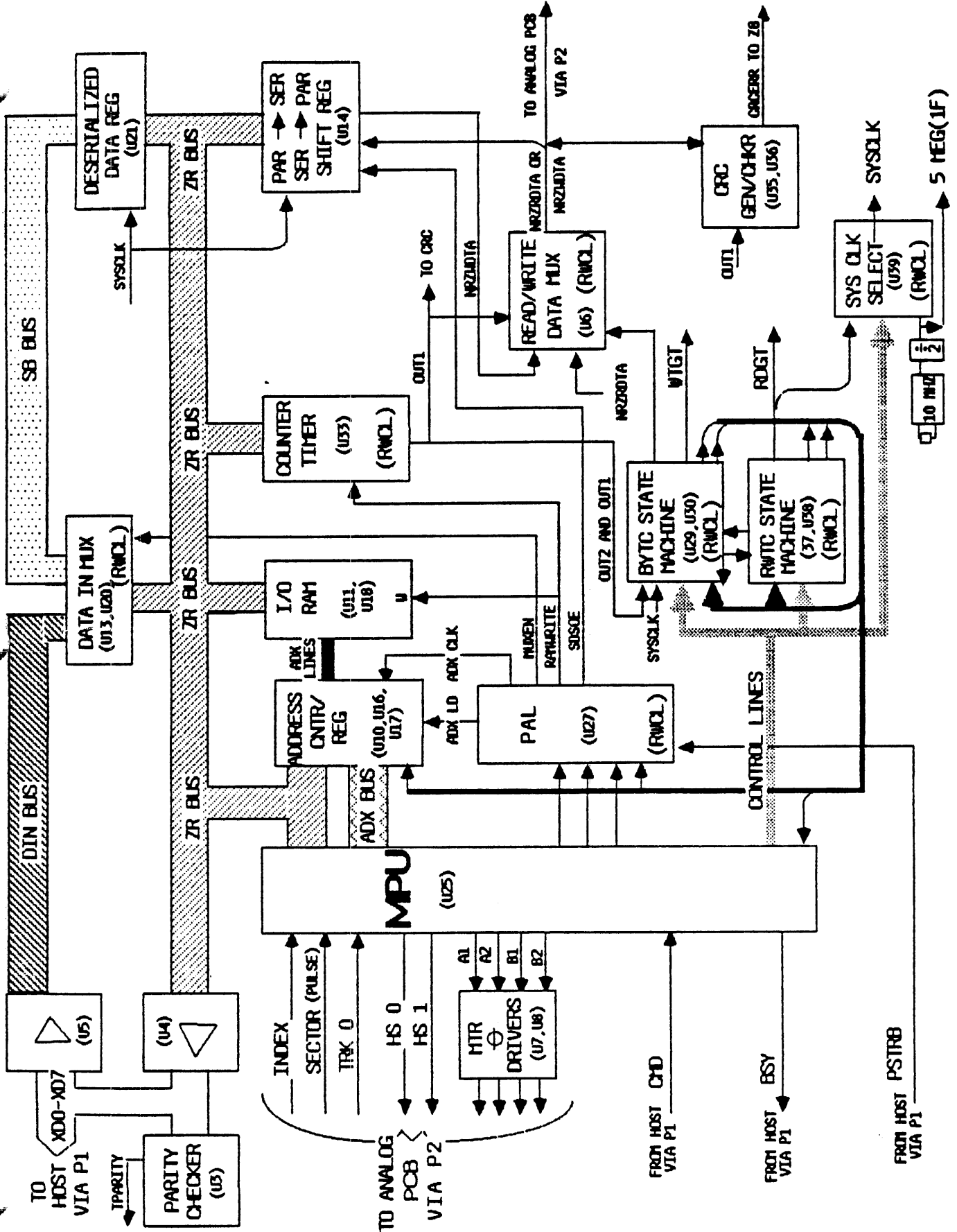
## Controller PCB Circuit Descriptions

29. The 16 bytes of target sector header information were stored in 16 memory locations of RAM. When the Address Counters increment past 16, A4 goes high, which signifies to the State Machine that a complete sector header has been checked and must be OK because the DATA signal must have remained low.

Signal A4 causes the State Machine to advance to sequence 5 or 6, depending on whether DRW is high or low, which depends on which operation the Host requested.

30. If DRW is high, the State Machine will go to sequence 6 for a Read operation. If DRW is low the State Machine will go to sequence 5 for a Write operation.

CONTROLLER PCB BLOCK DIAGRAM



## 3. Operations

The first part of all operations is the Check Header function (previously described). The following discussions deal with each of the three Pro-File operations after the Check Header function has been performed, which is after sequence 7 of the Read/Write control circuitry.

Once the Seek to the target track is confirmed, and the Z8 has a reference on where the target track is, the Z8 will condition the circuitry for the execution of an operation a number of sectors before the target sector, called the sector interleave (because the data come off the disk too fast for the circuitry on the Controller PCB to process the target sector's header).

The sector interleave is specific to the Host operating system using the Pro-File and to the operation being performed.

After the sector interleave, when the sector pulse for the target sector occurs, the Z8 enables the control logic to activate the circuitry for the operation requested.

### 3.1.1 Read Operation General Explanation

During a Read operation, after the Check Header function, NRZDTA enters through the Read Data MUX into the Deserializer.

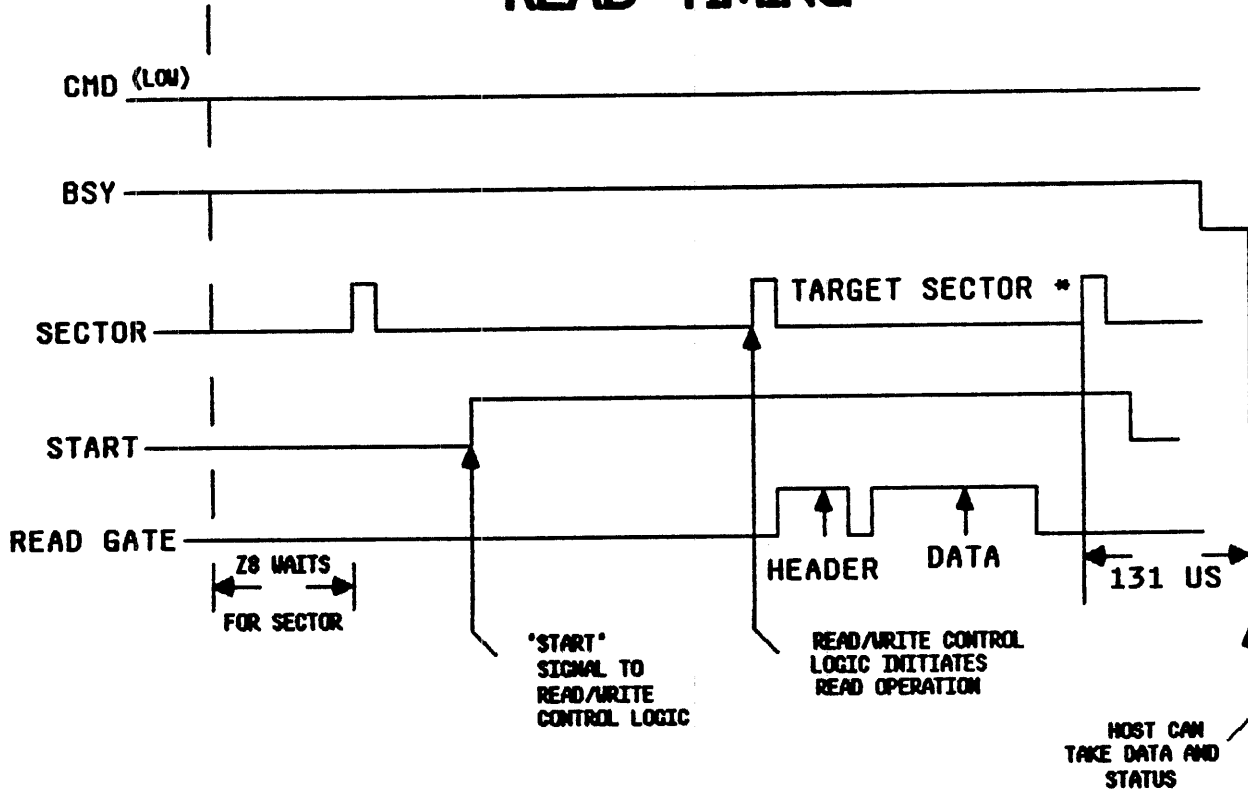
In the Deserializer, NRZDTA is converted to parallel bytes, and then transferred to the Deserialized Data Register, held momentarily, and gated through the Data In MUX to the RAM.

When the sector (block) is complete, the control logic tells the Z8 to lower the BSY line. It does, and then the Host uses PSTRB to strobe the data out of RAM through the output buffer to the Host interface PCB.

The RAM address counter has been set to the beginning of the data, and each strobe sent by the Host increments the Address Counters to the next address.



## READ TIMING



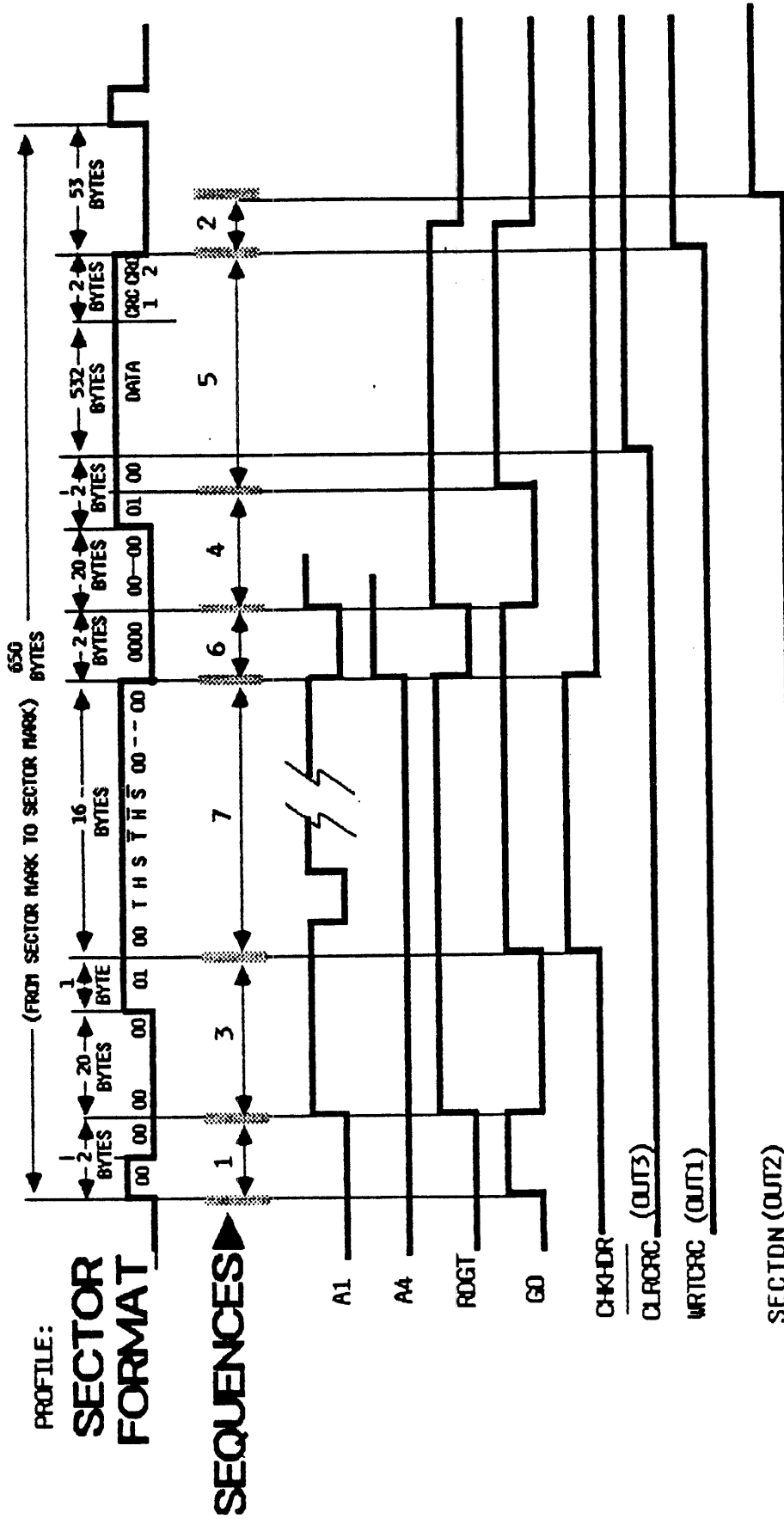
IF THE HEADER READ, IS NOT FROM THE TARGET SECTOR, THE HARDWARE CONTINUES TO READ SECTOR HEADERS UNTIL THE TARGET HEADER IS FOUND. BSY, AND START REMAIN HIGH.

Refer to the Controller PCB schematic at the end of this section for the following discussion.

### 3.1.2 Read Operation Component Explanation

1. As can be seen in the State Machine Sequence diagram after sequence 7 (the end of the Check Header function), if DRW is high (indicating the command bytes from the Host specified a Read operation) and A4 goes high (indicating all 16 bytes of the sector header field have been checked), the State Machine will advance to sequence 6.
2. Sequence 6 holds the Read/Write control circuitry in a wait state during the first two bytes of the sync byte field preceding the data field. These first two bytes can contain spurious data that could cause an error.
3. Because RDGT is not produced in sequence 6, the System Clock Selector U31 and U32 selects clocks from the crystal oscillator.
4. After two bytes of these clocks have been received, the A1 signal from the Address Counters goes true, to pin 5 of U29. This causes the BYTC (Byte Control) State Machine to produce ENDCOUNT out of pin 10 of U30, putting the State Machine in sequence 4 (as shown in the State Machine Sequence diagram).
5. Sequence 4 allows time for the VCO on the Analog PCB to sync to the sync byte field. While this is going on the Controller PCB is waiting for data (in this case the data field). In sequence 4, the RDGT signal (pin 7 of U38) is generated by the State Machine. This signal goes to the Analog PCB to enable it to convert the analog signal from the HDA head into NRZ data (NRZRDTA) and to generate RDCLKs in sync with this data. RDGTA also goes to the System Clock Selector U31 and U32 to select RDCLKs as the system bit clock.
6. Because the GO signal is low again at the beginning of sequence 4 the Deserializer chip (U14) is reset. This condition causes a low output from pin 17 of U14, which goes to pin 13 of the Exclusive Or in U28.

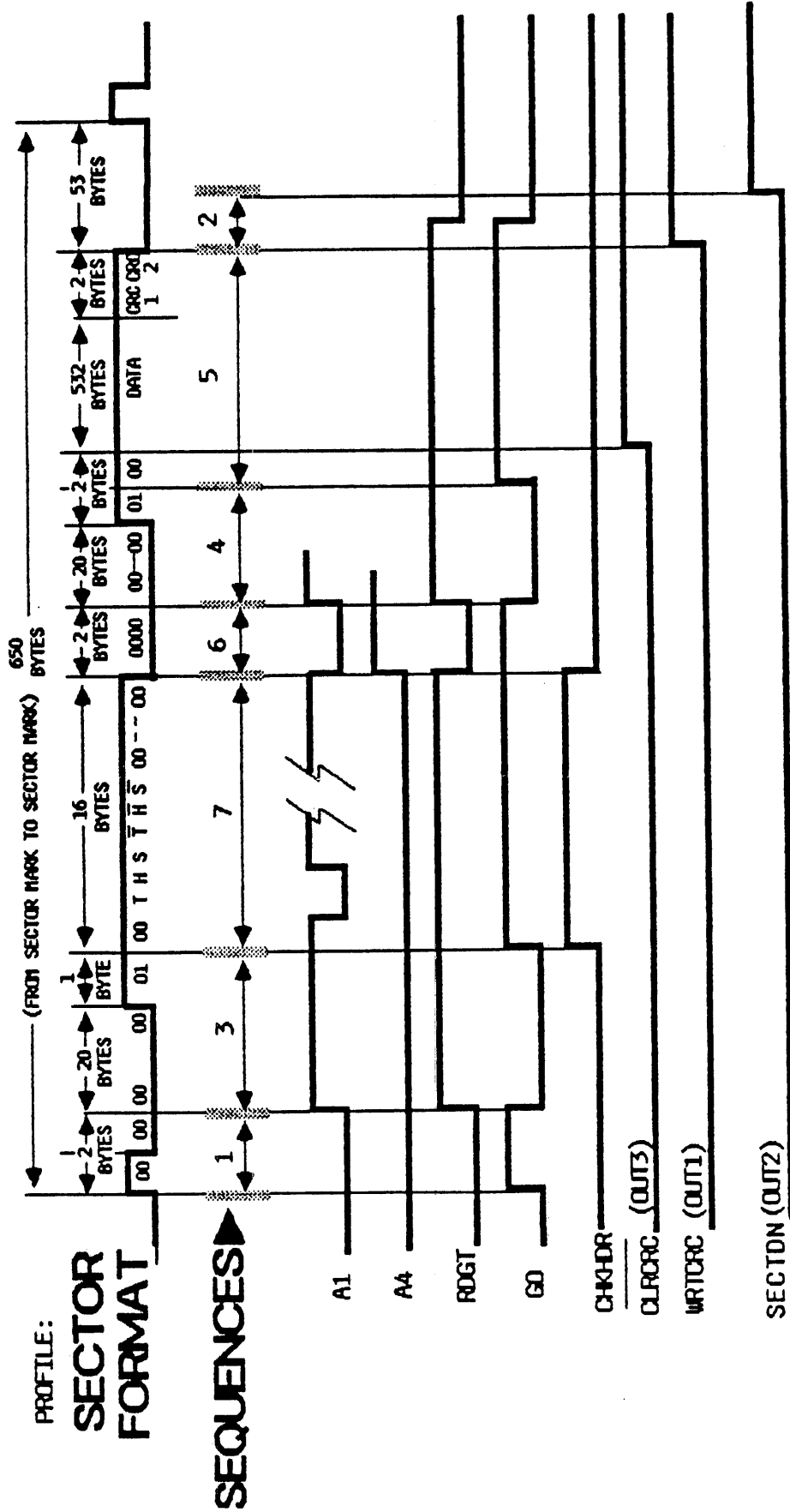
# READ SEQUENCE TIMING



## Controller PCB Circuit Descriptions

7. Pin 12 of U28 is NRZRDTA. At this point in reading the sector, NRZRDTA should be all 0's (because the sync bytes are all 0's), so pin 12 should be low, which, along with the low pin 17, results in a low out of pin 11 of U28.
8. Pin 11 remains low until the sync byte just before the data field (which contains a 1) occurs; now the inputs to the Exclusive Or are different, making DATA signal on pin 11 high .
9. As can be seen from the State Machine Sequence diagram, the high DATA signal is the condition that causes the State Machine to advance to sequence 5.
10. Sequence 5 generates either RDGT or WTGT, depending on the level of DRW. If DRW is high, the command bytes from the Host have stipulated a Read operation, so RDGT will remain high. If DRW is low, WTGT will occur. Sequence 5's function during Read is to read the data field from the target sector on the HDA.
11. The GO signal goes high at sequence 5 to enable the Divide-by-8 Counter U22 to begin counting RDCLKs again and to produce QC pulses once per byte to decrement the counting registers in the Programmable Counter/Timer (U34).
12. Since NRZRDTA is in serial form coming from the Analog PCB, it must be deserialized and sent to RAM in bytes. This is done by the Serial/Deserial Shift Register U14. NRZRDTA comes in to pins 5 and 6 of the Read Data MUX U6. Because this is a Read operation, pin 2 is low, enabling the Read Data MUX to pass serial NRZRDTA to pin 11 of the Serial/Deserial Shift Register U14.
13. The NRZRDTA is clocked into the Serial/Deserial Shift Register U14 with RDCLKs at pin 12. At the phase 0 following a byte of data, the contents of the Serial/Deserial Shift Register U14 are enabled to merge onto the ZR bus by the signal SDSOE from pin 13 of the PAL U27. This timing relationship can be seen on the State Machine Phase diagram (shown in the Check Header function circuit description).

# READ SEQUENCE TIMING



## Controller PCB Circuit Descriptions

14. LDSBF (from pin 12 of U29 the State Machine) also occurs at phase 0, to load the byte from the ZR bus into the Deserialized Data Register U21.
15. Once U21 contains a byte of received data, its contents merge on the SB bus. The Data In MUXers U13 and U21 are enabled by the high MSEL1 signal from the Z8 to pin 1 to select the SB bus, and so pass the byte to the data input of the RAM.
16. In sequence 5, the RWTC State Machine produces SSTRBs each phase 1 from pin 15 of U38. This happens once per byte, triggered by the inputs from the Divide-by-8 Counter U22.
17. During sequence 5, the PAL U27 generates the low RAMWRITE signal, on pin 16, to the RAM each time SSTRB occurs. This enables the byte of information from the Data In MUXers U13 and U21 to be stored into the address currently being selected by the Address Counters.
18. The SSTRBA signal also increments the Address Counters U16, U17, and U10 after storing each byte received from the disk.

### CRC Operation

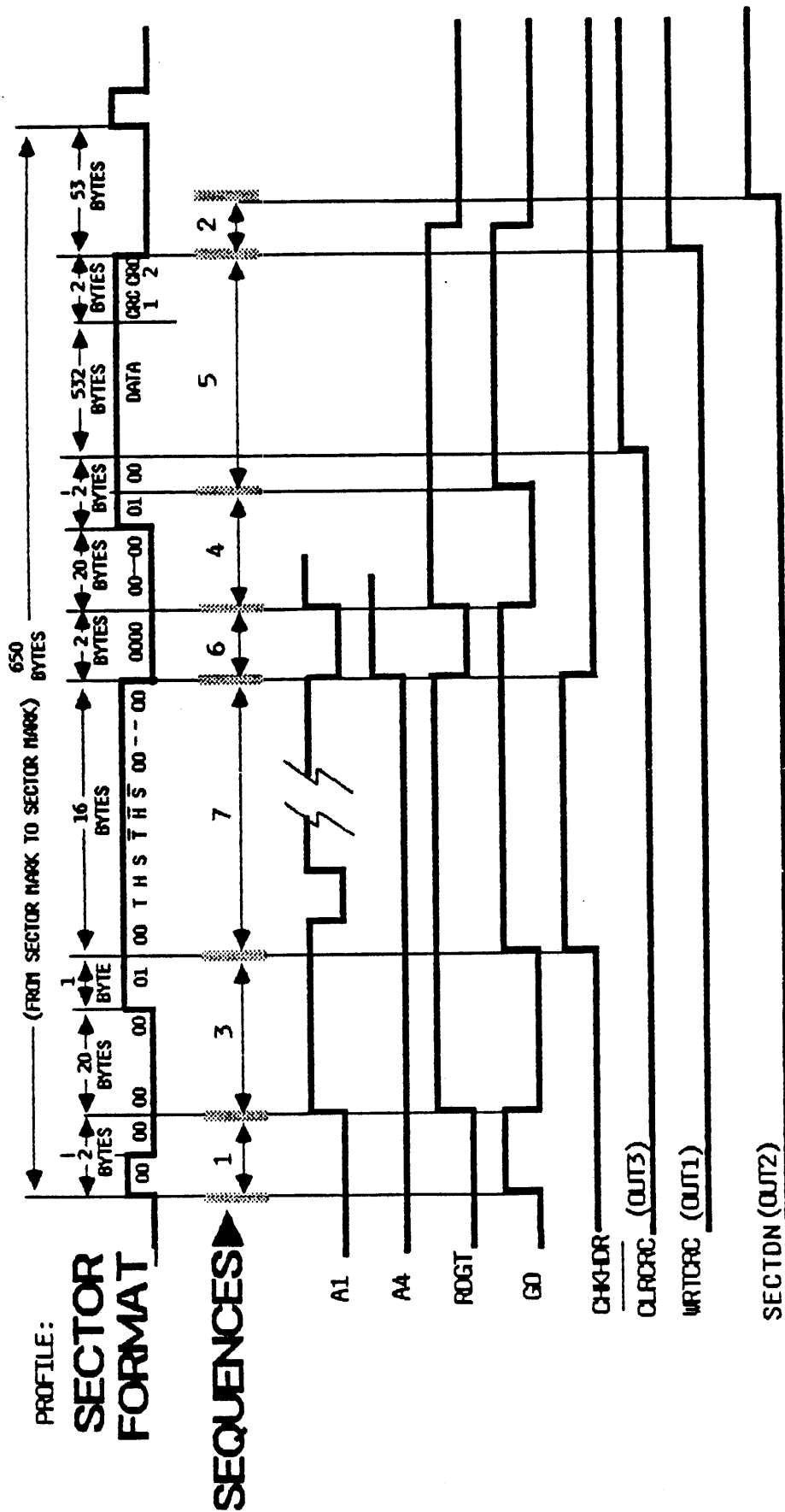
19. Prior to sequence 6, during the Check Header function, the Z8 reprogrammed the Programmable Counter/Timer (U34) so that:
  - a. OUT1 register contained 553.
  - b. OUT2 register contained 555.
  - c. OUT3 register contained 19.

The Programmable Counter/Timer (U34) is enabled to decrement all of its registers each time an SSTRB occurs, but only while GO is high.

During the sequences of the first part of the Read operation (including the Check Header function), each of these registers is decremented by the following amounts.

Sequence	Amounts
1	2
7	16

# READ SEQUENCE TIMING



## Controller PCB Circuit Descriptions

This brings the amounts in each register to:

- a. OUT1 register contains 535.
- b. OUT2 register contains 537.
- c. OUT3 register contains 1.

20. The second byte received during the data field of sequence 5 is never data but instead is a 00. The GO signal is high for this byte, so the SSTRB generated during its reception also decrements the registers in the Programmable Counter/Timer (U34). This causes the OUT3 register to arrive at 0, causing CLRRC to go high on pin 1 of an Exclusive Or gate in U28.

NOTE: Although the three U28 gates inputting to the CRC circuit are shown to be exclusive Ors, they are being used as inverters.

21. The other input to this gate (pin 2) is constantly high. Having two highs causes the gate to output a low, removing the high reset on pin 4 of the CRC Generator/Checker U35.

22. NRZRDTA is going to pin 11 of the CRC Generator/Checker U35. This chip is now enabled to use its internal logic to process each received bit from the data field and reflect its CRC status with its output on pin 13. If an error occurs, pin 13 of the CRC Generator/Checker U35 will go high, setting the CRC Error FF U36, which produces the low CRCERR signal to pin 30 of the Z8.

The Z8 then knows it has faulty data, and will perform an error recovery routine. (For more information on the error recovery routines used in the Pro-File's firmware, refer to the Appendices section of this manual.)

23. The OUT1 register is also decremented by the second byte in the data field, bringing its contents to 534.

After the remaining 532 bytes of data, and the two CRC bytes are read from the data field, the OUT1 register completes its count causing:

- a. The CRC Generator/Checker U35 to freeze its status.
- b. The State Machine to generate ENDCOUNT and advance to sequence 2.





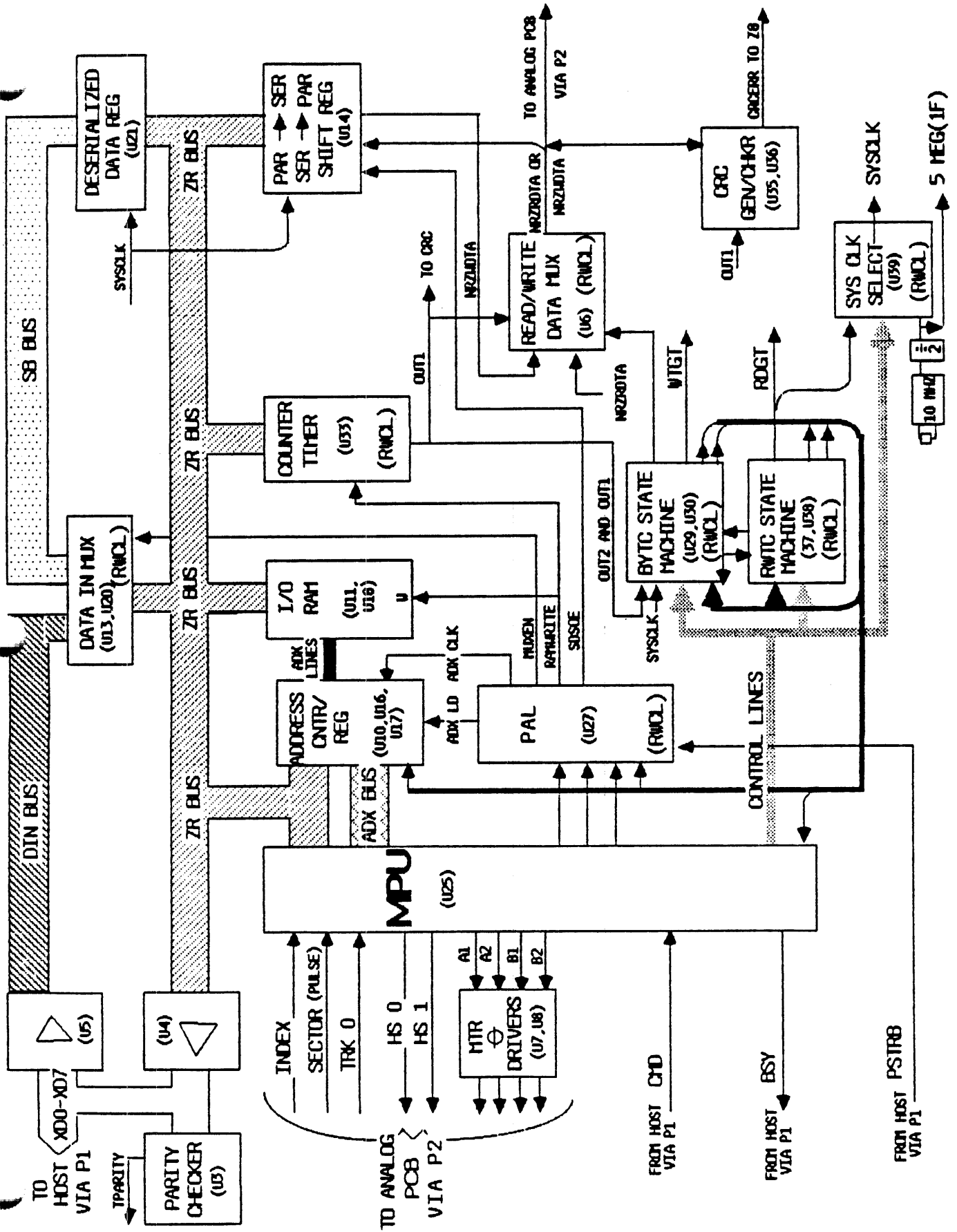
24. Sequence 2's purpose is to hold the Read/Write Control Logic in a static state until the Z8 is finished processing the CRC status. This happens when OUT2 decrements to 0, causing the State Machine to output the SECTDN pulse.

This pulse accomplishes two functions:

- a. It resets the Programmable Counter/Timer (U34).
- b. It goes to pin 31 of the Z8.

When the Z8 receives the SECTDN pulse, it samples the CRC status from U35 and, when finished processing, lowers the START signal, causing the Read/Write Control circuitry to reset to sequence 0.

CONTROLLER PCB BLOCK DIAGRAM



### 3.2.1 Write Operation General Explanation

There are 3 handshakes for the Write or Write/Verify operations.

After completing the Command Handshake (the first handshake), the Z8 conditions the Controller PCB logic to accept a block of write data from the Host.

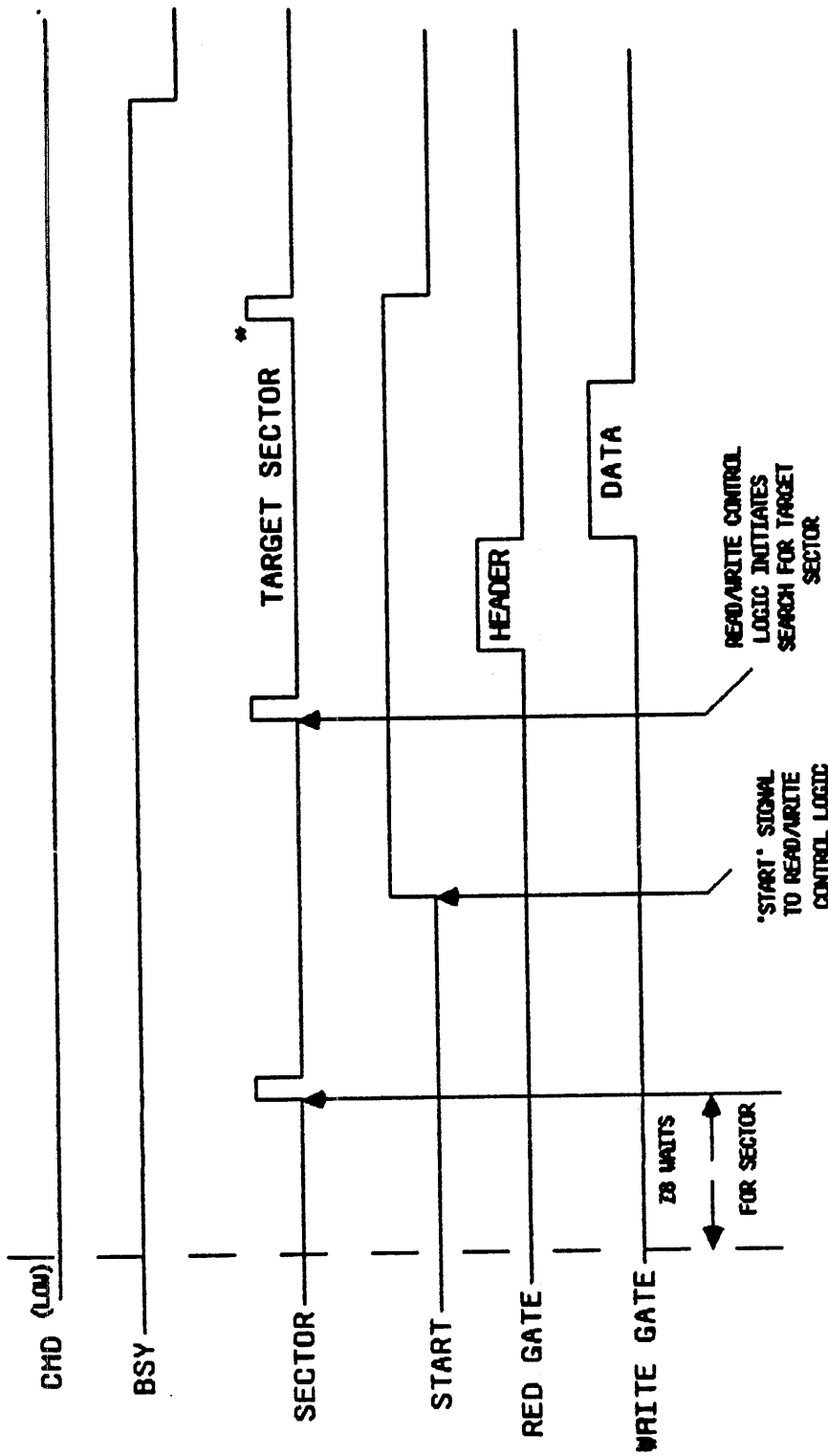
During the second handshake, the Host strobes each byte of data into the RAM with PSTRBs.

Then the Z8 and Read/Write Control Logic read the parallel write bytes out of the RAM to the Serial/Deserial Shift Register U14. U14 is then enabled to shift these bytes out in serial to the Analog PCB.

During a Write operation the WTGT signal enables the Analog PCB to convert this serial NRZ data to MFM data and then to an analog signal to be written on the disk surface. Once the Write is complete the Pro-File will go through yet another handshake.

The third handshake allows the Pro-File to send the completion status for the operation back to the Host.

# WRITE TIMING



\* THIS SECTOR PULSE IS TEMPORARILY SUPPRESSED BY WRITE OPERATION.

Refer to the Controller PCB schematic at the end of this section for the following discussion.

### 3.2.2 Write Operation Component Explanation

The following discussion explains the Write operation only so far as it differs from the Check Header function.

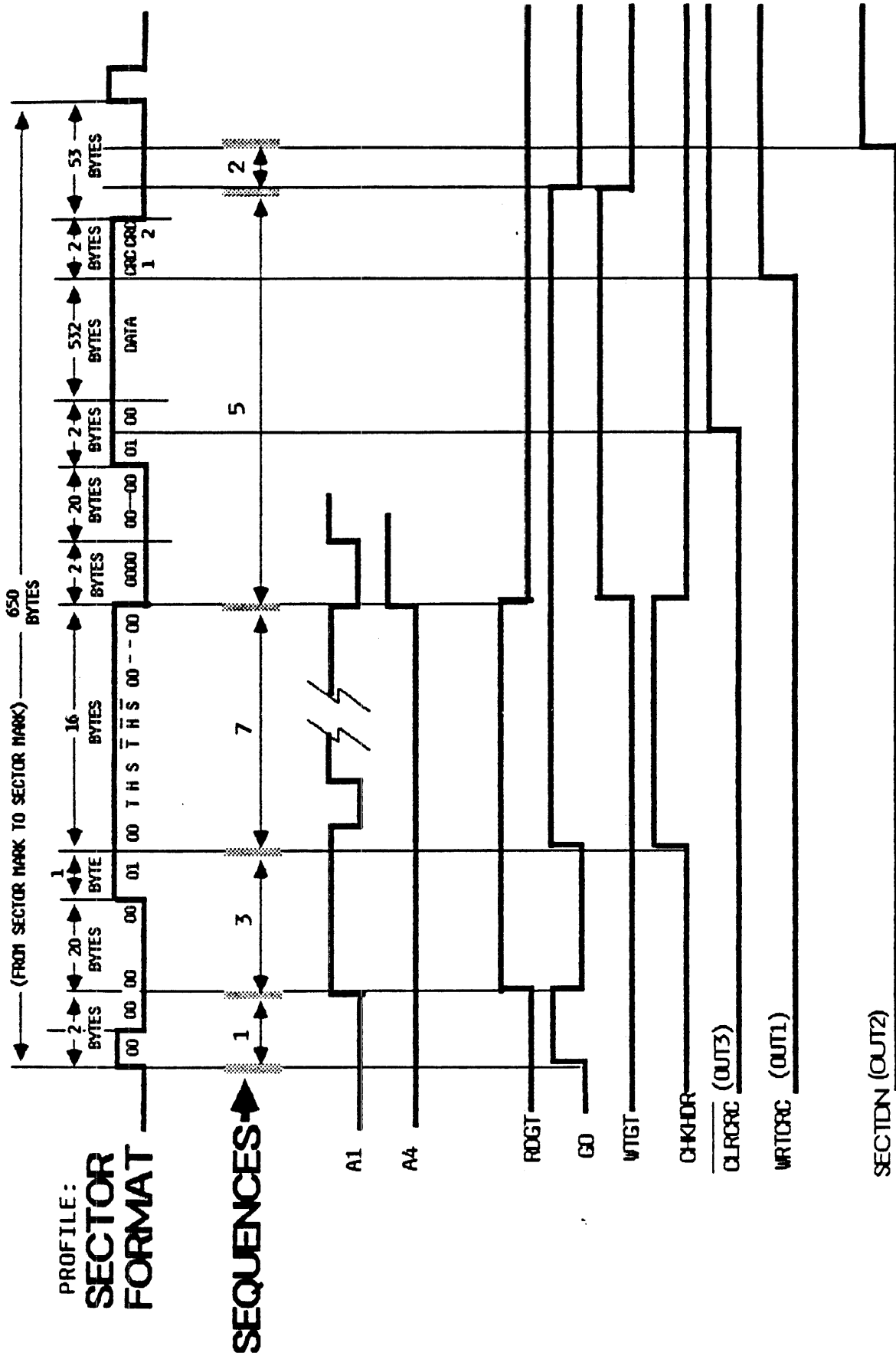
1. As can be seen in the State Machine Sequence diagram following sequence 7 (the end of the Check Header function), if DRW is low (indicating the command bytes from the Host specified a Write operation), and A4 goes high (indicating all 16 bytes of the sector header field have been checked) the State Machines will advance to sequence 5.
2. Sequence 5 will generate either RDGT or WTGT depending on the level of DRW. IF DRW is low, that means the command bytes from the Host stipulated a Write operation so WTGT will go high.

If DRW were high RDGT would occur. Sequence 5's purpose during a Write is to read the parallel write data out of RAM (this data was sent to the Pro-File during the second handshake of a Write operation), convert it to serial NRZ write data, and send it to the Analog PCB in sync with the system clock from the crystal oscillator.

3. Because RDGT is not being generated the System Clock Selector U31, and U32 will select the output from the crystal oscillator to use as the system bit clock for the rest of the Write operation.
4. The WTGT signal, pin 5 of U30, is generated by the State Machine as a result of being in sequence 5. This signal goes to the Analog PCB to enable it to convert the serial NRZ write data to serial MFM data, and then to an analog signal for the selected head to store on the disk surface.
6. After sequence 7 the Address Counters will be set to the RAM address of the first byte in the data block to be written.

The write data block in RAM is composed of 22 bytes of zeroes, then a sync byte containing a 1, then another zero byte, and then 532 bytes of data. During sequence 5, each write byte is read sequentially from the RAM.

# WRITE SEQUENCE TIMING



7. Because the State Machine is in sequence 5, the Divide-by-8 Counter U22 will be enabled by the high GO signal to count system bit-clocks (since RDGT is low the System Clock Selector U39 will select the clocks from the Controller PCB crystal oscillator).

Each QC output from the Divide-by-8 Counter U22 will produce an LSDS output from pin 12 of U29 in the State Machine to pin 19 of the Serial/Deserial Shift Register U14 enabling it LOAD a byte of write data from the ZR bus. As can be seen on the State Machine Phase diagram (shown in the Check Header function circuit description) LSDS occurs at phase 7 of a byte to load the next byte from the bus.

8. In sequence 5 the RWTC State Machine will produce SSTRBs from pin 15 of U38. This happens once per byte as a result of the inputs from the Divide-by-8 Counter U22.
9. As can be seen on the State Machine Phase diagram, SSTRBA will be generated at phase 1 following the generation of LSDS. And so the SSTRBA signal increments the Address Counters U16, U17, and U10 after the Serial/Deserial Shift Register U14 has accepted one from the ZR bus.
10. Prior to sequence 5 of the Write operation, during the Check Header function, the Z8 reprogrammed the Programmable Counter/Timer (U34) such that:
  - a. OUT1 register contained 573.
  - b. OUT2 register contained 575.
  - c. OUT3 register contained 39.

Programmable Counter/Timer (U34) is enabled to decrement all of its registers each time an SSTRB occurs, but only while GO is high.

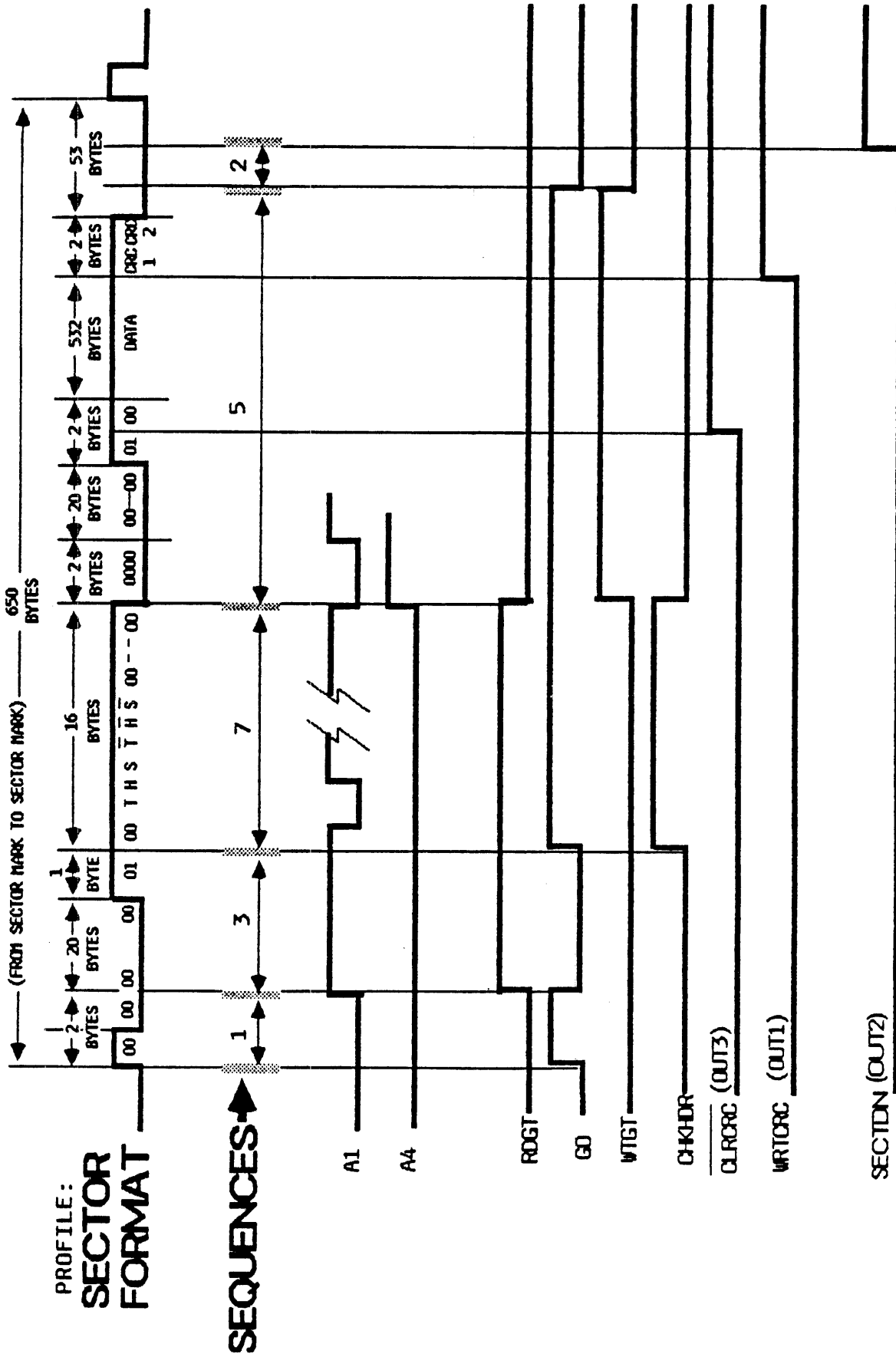
During the sequences of the first part of the Write operation (including the Check Header function), each of these registers was decremented by the following amounts.

Sequence	Amounts
1	2
7	16

- This brings the amounts in each register to:
- a. OUT1 register contains 555.
  - b. OUT2 register contains 557.
  - c. OUT3 register contains 23.



# WRITE SEQUENCE TIMING



**CRC Operation**

11. After the 22 sync bytes (which were zero's), and the "one" sync byte (which was a one), have been read out of RAM the OUT3 register will be decremented to 0, and the OUT1 register to 532.

The OUT3 register reaching 0 causes a high from pin 15 of U34, removing the high Reset signal to pin 4 of U35 the CRC Generator/Checker. This chip is now enabled to process write data bits to produce 2 unique CRC bytes for the 532 bytes in the data field.

12. Meanwhile the Read Data MUX U6 is enabled by the high WTGT signal to select the serial output of the Serial/Deserial Shift Register U14 at pin 19.

This serial write data is sent up to pin 11 of the CRC Generator/Checker U35. When 532 bytes have been counted, the OUT1 output from the Programmable Counter Timer U33 goes high causing the FRZN/WRTCRC signal to pin 5 of U28.

NOTE: Although the 3 U28 gates inputting to the CRC circuit are shown to be exclusive Ors, they are being used as inverters.

13. The resultant low on pin 10 of U6 causes the CRC Generator/Checker U35 to change modes to freeze the CRC generator, and clock out the 2 CRC bytes as NRZ Write data.
14. The OUT1 signal also goes to pin 19 of the BYTC State Machine to produce ENDCOUNT causing the State Machine to produce SECTDN and advance to sequence 2.
15. SECTDN goes to pin 31 of the Z8 to tell it that the processing of the sector is finished, and sequence 2 simply holds the Read/Write Control circuitry until the Z8 can process the SECTDN signal and drop the START signal. Otherwise spurious data could be stored in RAM.

### 3.3.1 Write/Verify Operation General Explanation

The Write/Verify operation is a combined Write and Read. The data comes from the Host in the same way as it does for a Write.

When the Write operation is complete the Z8 goes through a verification of the data written, much like a Read operation.

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## ANALOG PCB

### 1. General Explanation of the Analog PCB Write Circuits

For the following discussion refer to the Overall Block Diagram of the Analog PCB on the opposite page.

The Analog PCB serves as the interface between the Controller PCB and the Seagate HDA.

It consists of two main parts Write circuitry and Read circuitry.

The one Head Selector is shared for both Read and Write.

The Write circuitry consists of the following circuits:

- a. Non-Return to Zero ( ) to Modified Frequency Modulation (MFM) Write Encoder and Data Precompensator.
- b. Write Driver.
- c. Head Select Matrix.

#### 1.1 NRZ to MFM Write Encoder and Data Precompensator Circuits

Prior to any operation (Write or Read), the Z8 on the Controller PCB sends the head select matrix inputs to cause it to select one of the four heads (disk surfaces).

During a Write operation, serial NRZ WRTDATA (Non Return to Zero simply means the data signal will be high when a one and low when a zero with no clocks) is converted to MFM data by the MFM Encoder/Precompensator. (For information on Modified Frequency Modulation refer to the MFM explanation at the end of this discussion.)

The Write Driver converts the MFM write pulses to alternating head current on the selected head.

If the data is being written on an inside track (tracks 128 to 152), the MFM write transitions will be peak shift precompensated, and the Write current will be reduced from 24 ma to 19 ma.

The Write Driver and Head Select Matrix are covered in more detail later.

For information on Write Precompensation refer to the Write Precompensation explanation at the end of this discussion.



2. Component Explanation of the Analog PCB Write Circuits

Refer to the diagram on the opposite page for the following discussion.

Some minor component value changes exist from this drawing to the production version. But, the illustration should be adequate for training purposes. The component population of the Write circuitry is quite small. However, the PAL (programmed array logic-U28) makes up for that by having a large amount of logic.

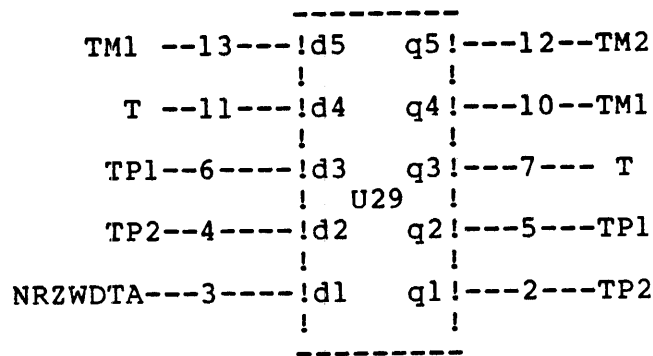
2.1 Clocking-

The 10MHz 2F signal is the master clock frequency from the crystal oscillator on the Controller PCB. It is divided to 1F (5MHz) by U2 (a simple divide-by-two stage). The 1F signal is the bit shift clock for the precompensation shift register. It is also used to keep the VCO synchronized to write data during the Write operation. The 2F signal provides the clock enable signals necessary to perform precompensation on the data as it is output from the PAL.

2.2 Precomp Shift Register U29

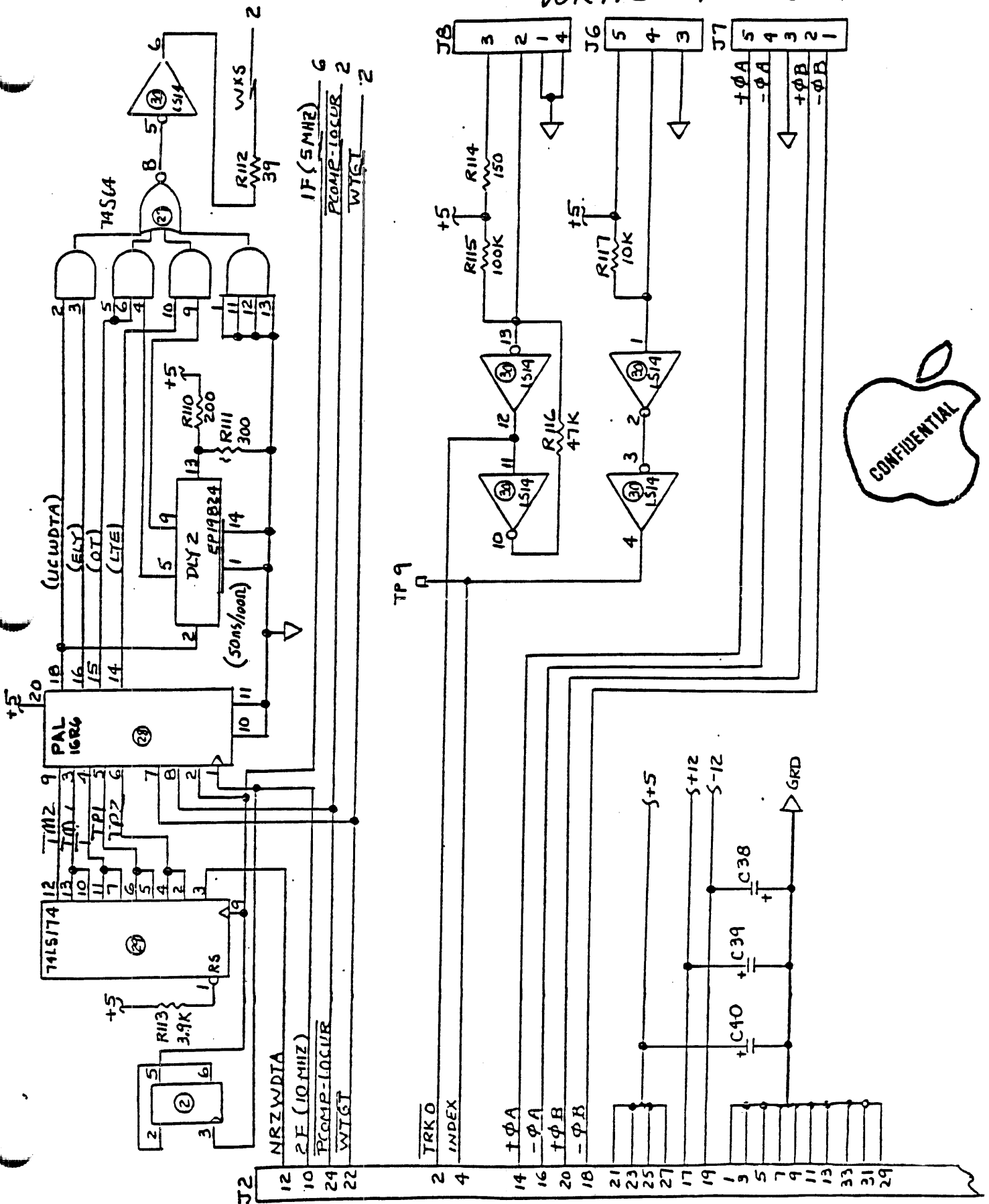
U29 has been externally wired into a shift register. Its output shift pattern provides five of the inputs to the PAL.

For clarity, the following is a sketch of U29 and its signals with the "in's" on the left and the "out's" on the right.



It makes things easier if you visualize the data stream in reference to the bit named "T". The TMx signals are what T was one or two clocks ago, and the TPx signals are what T will be in one or two clocks. The initial NRZ data is clocked into q1, the next clock places q1 at q2, and so forth. The whole intent is to give the PAL a window on the data stream to make the encoding and the early/late/ontime precompensation decisions discussed earlier.

WRITE PRECOMP





## Analog PCB Circuit Descriptions

### 2.3 PAL Chip U28

U28 is a custom array of logic designed specifically for this circuit. It consists of a huge array of AND/OR gates feeding each D input of its output register.

The PAL chip is involved in two functions:

1. To convert the NRZ digital stream into a stream of pulses conforming to the rules of MFM as stated earlier.
2. To provide the gating signals to advance, retard or leave alone the stream of write data pulses called "UCWDTA" (uncompensated).

As a bit is being processed through the PAL chip, its internal array of AND/OR gates receives inputs from the Precomp Shift Register U29, telling the PAL which bit combinations surround that bit.

This enables the PAL to determine when to generate a transition to convert it to MFM data and what type of precompensation (if any) to provide.

### 2.4 Precompensation Gating U27

UCWDTA goes to the input of a gate enabled with ELY (Early) and to a delay line DLY2, which delays the pulses approximately 15 ns per stage. The outputs of the delay line are partial enables to the OT (Ontime) and LTE (Late) gates respectively.

If there is no precompensation, (such as when writing to the outer tracks), the signal OT gates the first delayed data line to the WXS line.

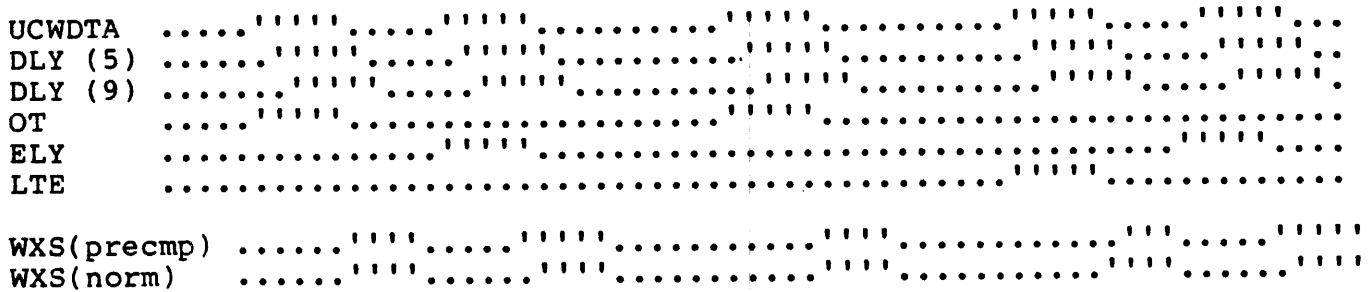
If precomp'ing determines that the data transition needs to be advanced, then the ELY signal will gate UCWDTA to the WXS line; and if the signal needs to be retarded, the signal LTE will gate the second delay of data to the WXS line.

DLY2 provides the amount of delays needed for each type of precompensation. Only one signal (UCWDTA, ELY, OT, or LTE) can be true at any one time.



**2.4 Precompensation Gating U27 (continued)**

The following timing diagram might help make this more clear.



NOTE: this diagram is for training purposes and does not necessarily conform to the rules of precomp....OK?

The leading edge of the WXS signal is the working edge that toggles the WXS FF. The slight shift of timing between the precomp and unprecompensated signal is enough to increase Read data recovery by several magnitudes.

**2.5 Miscellaneous Circuits U30**

These drivers shape the TRACK 0 sensor signal and the INDEX pulse from the HDA. The Track 0 circuit forms a noise latching function too (the source signal is pretty ragged).

**2.6 Write Current Gating U1, U2, U3, U31**

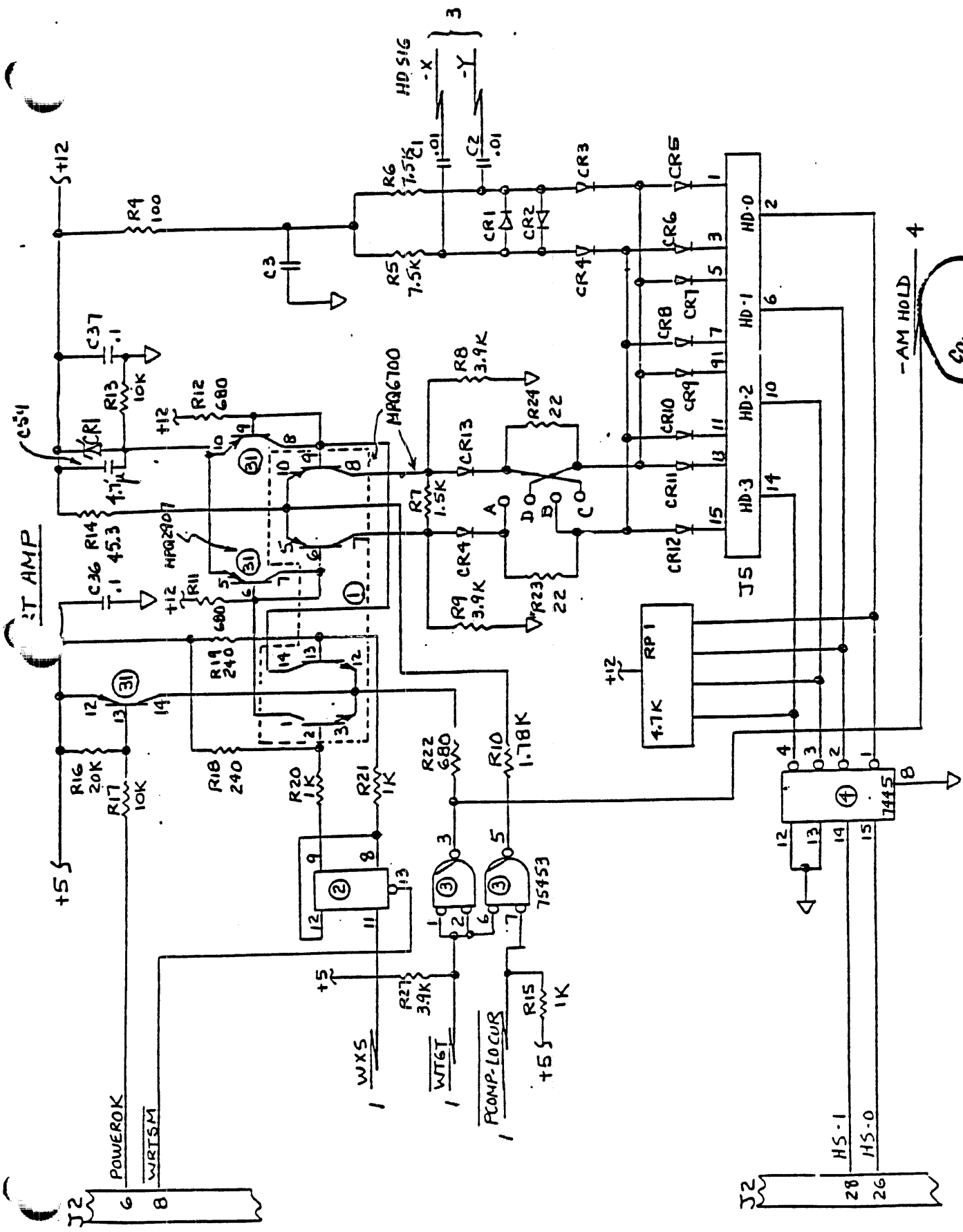
Each WXS pulse from the precomp gating circuit toggles the WXS FF, U2. The result is a divide by two function.

The output levels of the WXS FF are level shifted by the first set of transistors in U1.

The remaining transistors comprise a constant current-switching network. These transistors are turned on and off depending on the state of the WXS FF.

During Formatting, at the end of every sector the Z8 on the Controller PCB directs the Analog PCB to write a sector mark. It does this by putting a constant low on pin 13 of the WXS FF to clamp it in the reset state for a 10-byte period.

Each time this happens, the heads output a DC level (no transitions) for a field (10 bytes long), creating a sector mark.



## Analog PCB Circuit Descriptions

### 2.6 Write Current Gating (continued)

A string of zeros would not create the DC level because they would be converted by the MFM encoder to a 5 MHz signal at the heads.

The Z8 causes WTGT to go low and turns on the current switching circuit when it wishes to perform a Write operation.

WTGT (Write Gate), when inactive (high), kills both sides of the level shifter and, therefore, turns off both sides of the current source, effectively killing all write current.

The signal PRECOMP-LOCUR is produced by the Z8 to cause a reduction of write current to the heads when writing to the inner tracks (128 to 152).

Normal write current is about 24 ma. But, in the inner tracks it is reduced to slightly less than 20 ma because the bits are packed closer together.

The POWEROK signal is generated by the power supply. If it goes low that means that the power supply has detected a power problem.

If the POWEROK signal does go low, this biases pin 13 of a transistor in U31 to turn it on inhibiting any write from taking place.

### 2.7 Head Selection U4

Head selection is done by U4 (7445, one of ten decoder). The signals HS0 and HS1 are code outputs from the Z8 to select the proper head (00 selects head 0, 01 selects head 1, 10 selects head 2, and 11 selects head 3).

Only one head can be selected at a time. The heads are center tapped, and the center is connected to the 7445 to create a current path for Reading or writing.



### 3. GENERAL EXPLANATION OF THE ANALOG READ CIRCUITRY

The following circuits are included in the Read circuitry:

1. Preamplifier and Automatic Gain Control (AGC).
2. Read Detector and Sector Mark Detector.
4. Phase Locked Loop (PLL) consisting of:
  - a. Phase Detector.
  - b. VCO Charge Pump.
  - c. Voltage Controlled Oscillator.
5. MFM to NRZ Read Decoder.

During a Read operation, the preamplifier amplifies the low level (.6 to 2.0 mV) signal from the selected head to a 200 mV.

The analog read signal is then filtered and amplified to a fixed 1.0 V output signal by the AGC circuit.

This analog read signal is fed to the differentiator and gated detector to derive the MFM read pulses.

The PLL (Phase Lock Loop) synchronizes its VCO to the MFM read pulses and provides the clock for the MFM to NRZ data converter.

The serial NRZ data and clock are sent back to the Controller for deserialization.

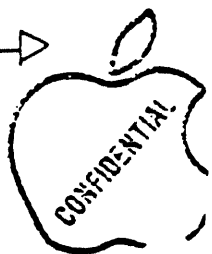
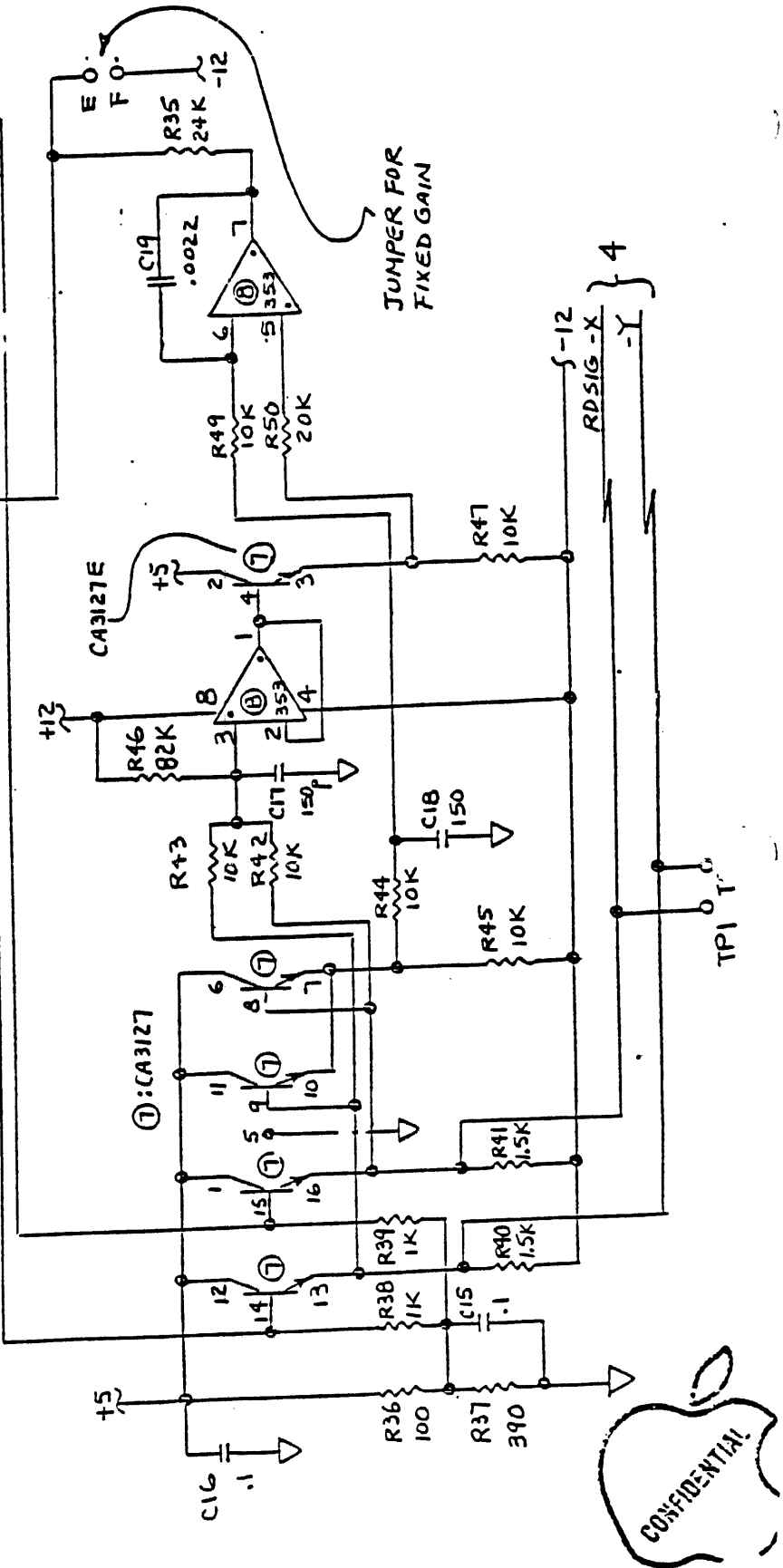
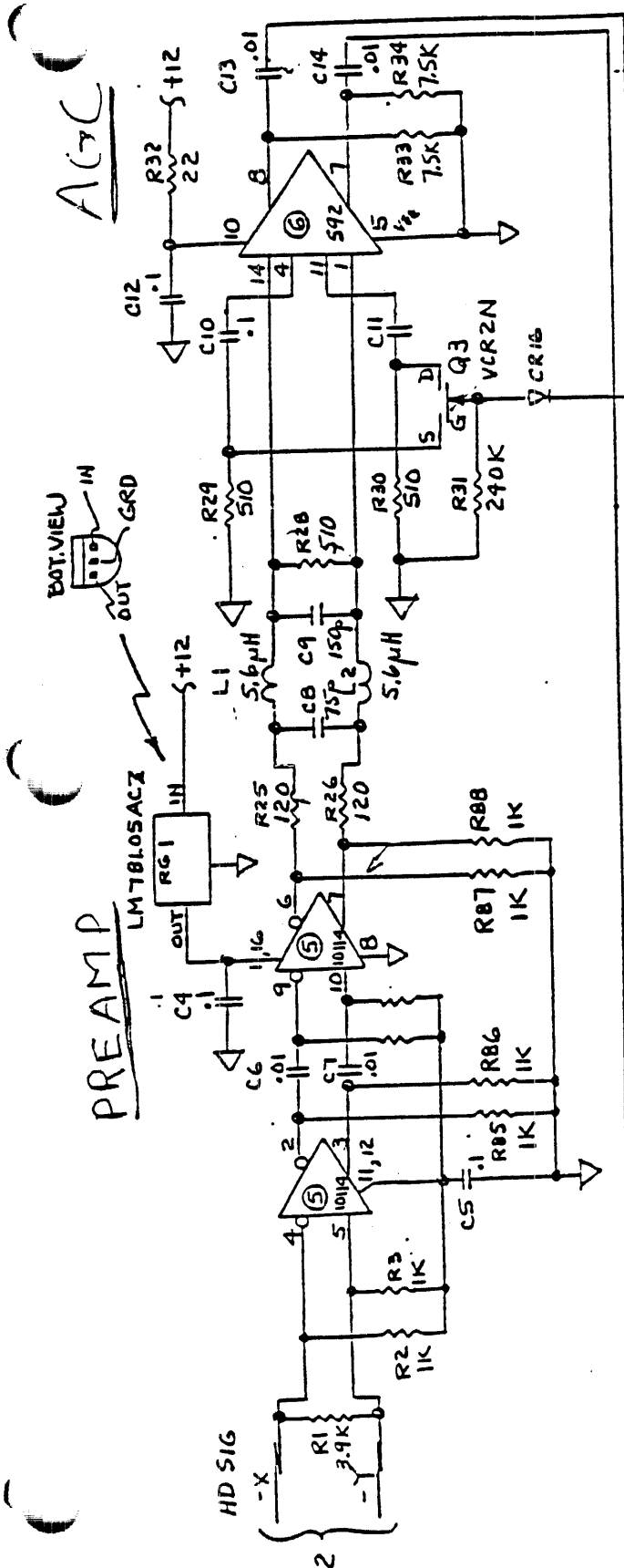
During format operation, when the initial sector identifier information is written on the disk, sector boundaries are written as DC-erased 10 byte fields.

During a Read operation, the sector boundary detector looks for the absence of Read signals for about 10 ms (to detect the DC-erased 10 byte field). When it detects one, it sends a sector pulse to the Z8 on the Controller PCB.

AC

BOT. VIEW  
IN  
OUT  
GRD

PREAMP





#### 4. Component Explanation of the Analog Read Circuitry

##### 4.1 Analog Preamplifier, and AGC (Automatic Gain Control) Circuits

The Read circuitry is always on. However, because of the amplitude of the write signal through the heads, it goes into saturation during the Write operation and does not reliably recover the data.

During Reading (not writing), the selected head develops a signal on the -x -y lines.

This signal is about 1 mv and cannot usually be seen with conventional techniques.

Probing dampens the signal and induces so much noise that the signal is obliterated. So don't expect to see data directly from the heads.

The read signals from the head are brought to the first stage preamplifier U5.

The devices used here are ECL (Emitter Coupled Logic), a high speed logic family. Each stage of the preamplifier has a gain of 12.

This means that the approximate 1 mV head signal leaves the first stage at about 18 mV. The signal is amplified again, and leaves this stage at about 200 mV.

That's nice because the filter network (L1, L2, C8, C9) attenuates the signal about 60%.

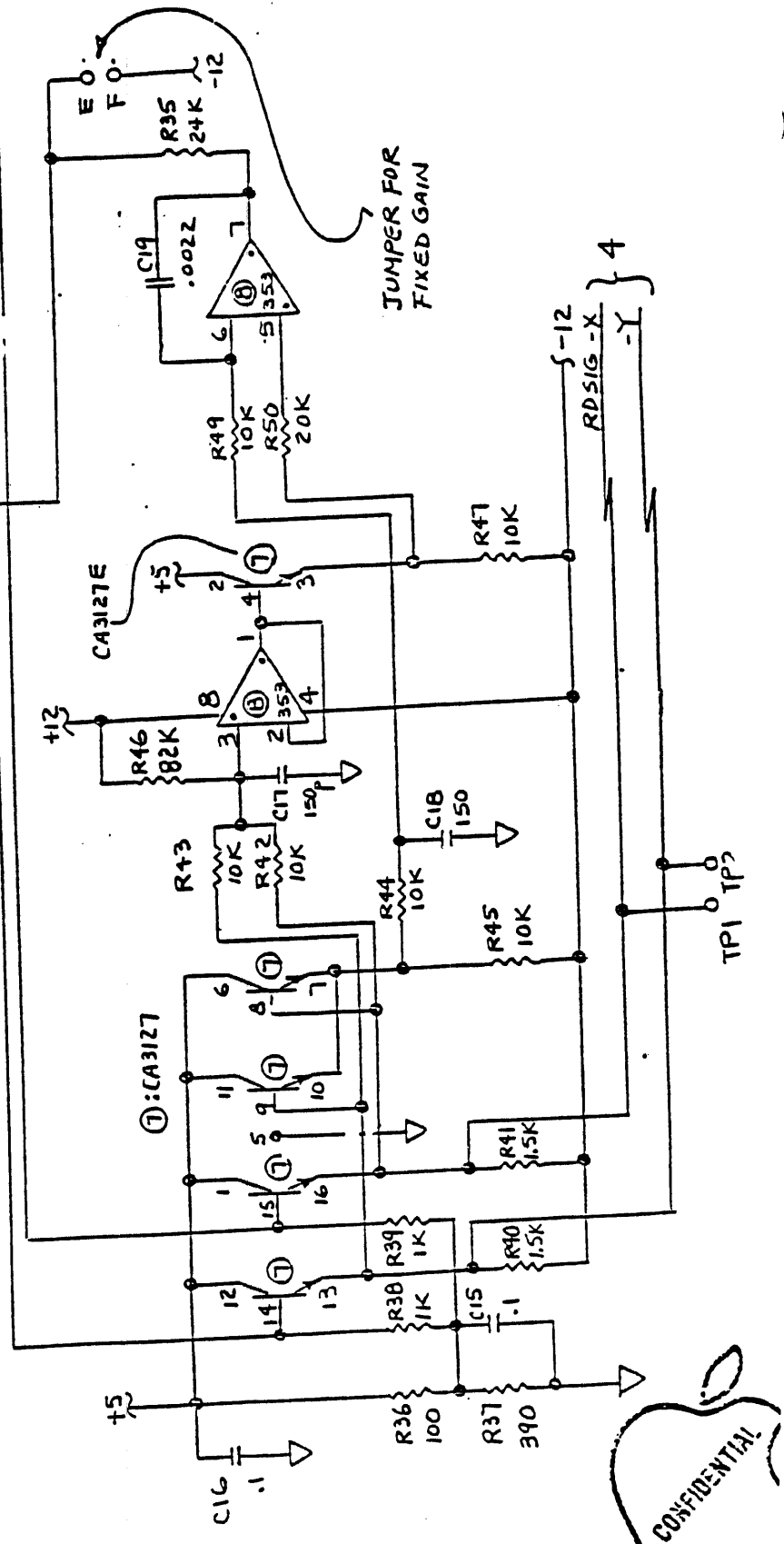
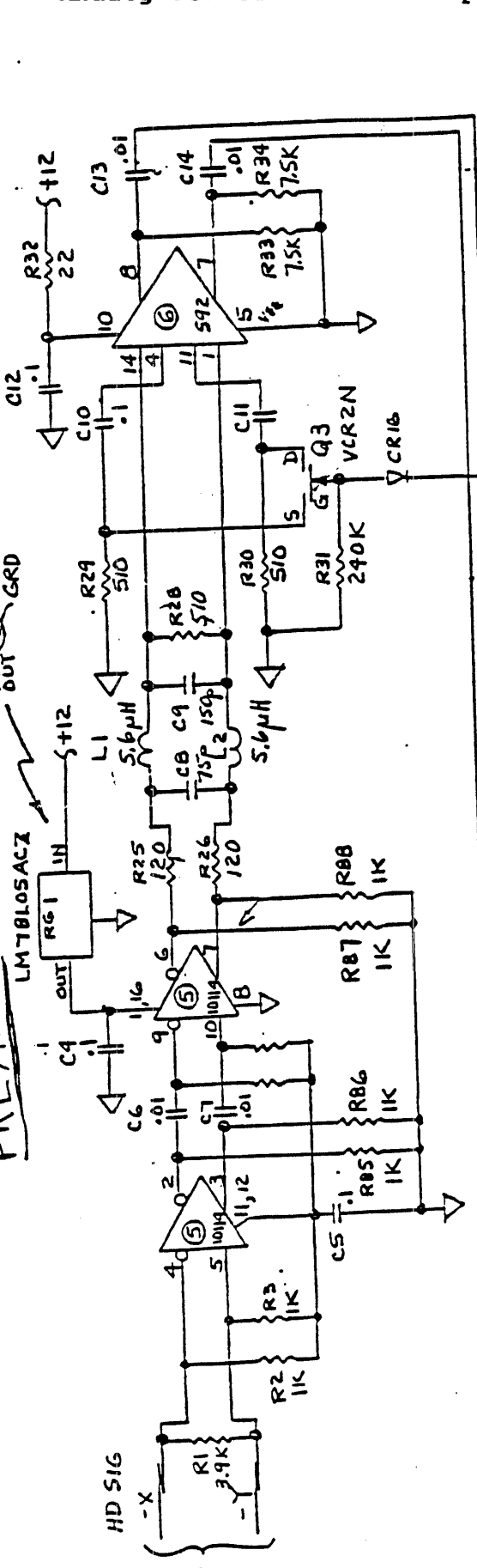
The analog read signal then enters the AGC (Automatic Gain Control) circuit. FET transistor Q3 controls the reference voltage to the amplifier U6.

The input to the gate of Q3 comes from the final output of the AGC circuit.

AGC

BOT. VIEW  
IN  
OUT  
GRD

PREAMP



CONFIDENTIAL

## Analog PCB Circuit Descriptions

If the output goes up, the bias on Q3's gate will cause it to increase the reference voltage on pins 11, and 4 of U6. This will cause the output of U6 to decrease.

If the output from the AGC circuit goes down, the bias on Q3's gate causes it to decrease the reference voltage on pins 11, and 4 of U6. This causes the output of U6 to increase.

The result of this process is that the AGC circuit is continually striving to regulate the input from the heads into a constant output level.

However, it takes a certain amount of time for this regulation to take place. That is why if you monitor TP1 or TP2 on the Analog PCB while Reading, you will see an increase in signal amplitude at the beginning of each sector.

During a sector mark, there is little amplitude at pin 7 of U8 (the final output of the AGC circuit), so Q3 is conducting, putting the reference voltage for U6 at a very low level.

The low reference voltages on pins 11, and 14 of U6 cause it to amplify at maximum gain.

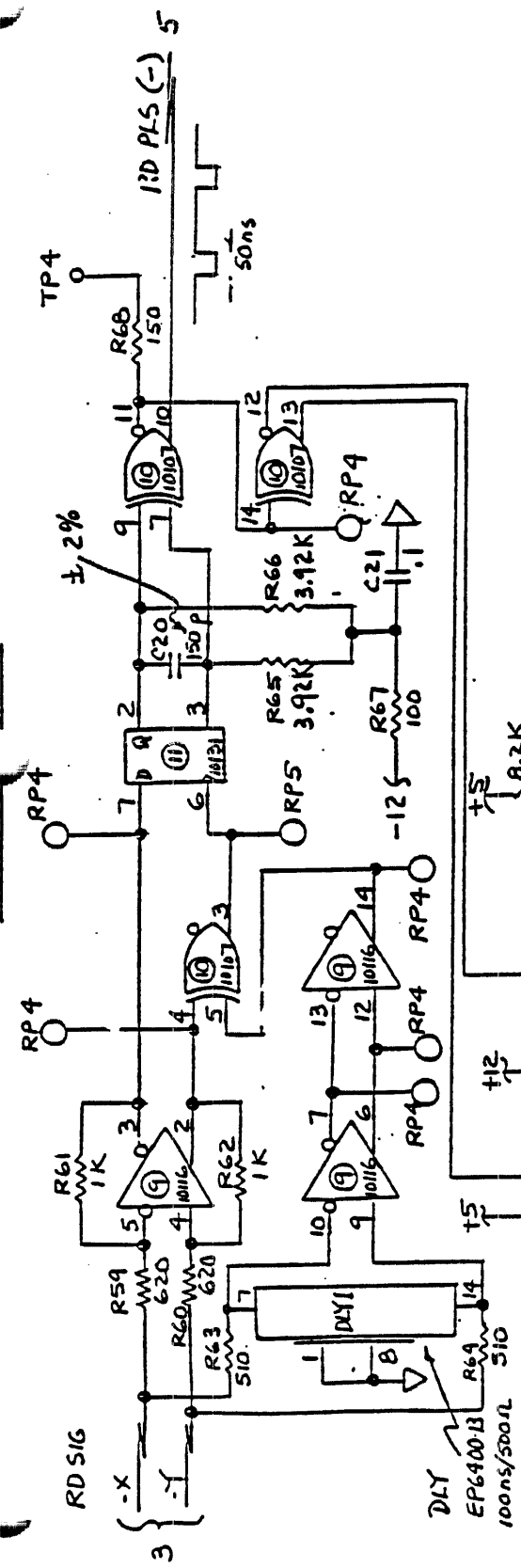
When the selected head starts receiving the next sector, U6 is still at maximum gain, so the sector read signal leaves U6 at a comparatively high amplitude.

Since the gain for the rest of the amplifiers in the AGC circuit is constant, this high output from U6 is amplified even further.

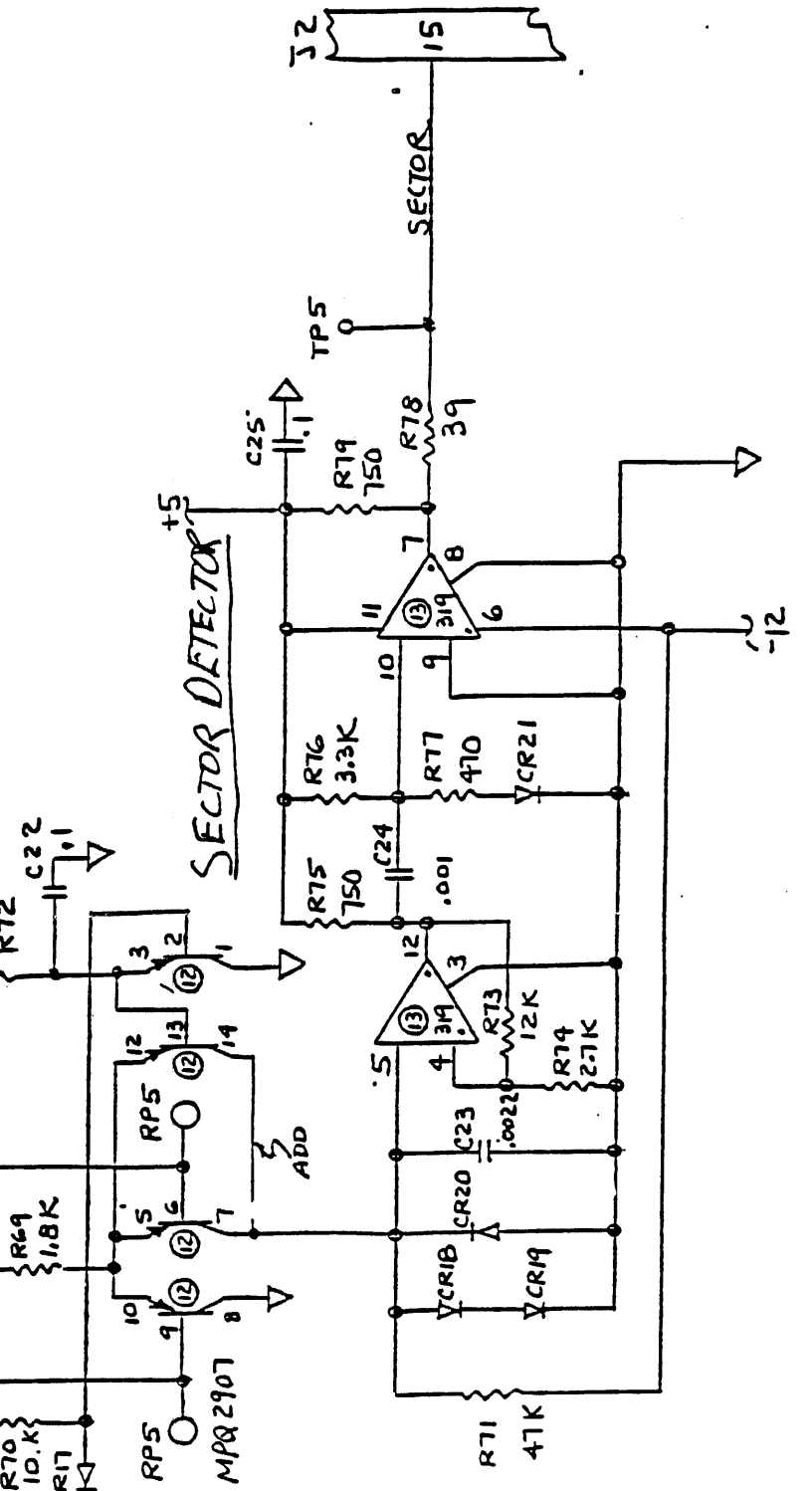
When pin 7 of U8 finally goes up, it causes Q3 to conduct less. This increases the reference voltage to U6, which decreases the output of U6, bringing the output of the AGC circuit back to its normal level.

This whole process occurs after every sector mark, and can be seen at TP1 and TP2 as a flare in amplitude at the beginning of each sector.

READ DETECTOR



SECTOR DETECTOR



#### 4.2 Read Detector, and Sector Detector Circuits

The Read Detector detects transitions in the analog MFM read signal and produces a 50 ns pulse for each one that occurs. The result is called digitized data.

U9, U10, and DLY1 set U11 every time a transition occurs.

C20, R65, and R66 make up an RC network that allows the set output of U11 to keep pin 9 of an Exclusive Or in U10 above its threshold and pin 7 below its threshold until the RC network's time constant is satisfied (TC = 50 ns).

This process produces a 50 ns digitized data pulse (called RDPLS) out of pins 10 and 11 of this Exclusive Or for every transition in the received analog signal.

(Refer to the timing diagram on page \* for an example of the timing relationship between the analog MFM read signal, digitized data, MFM data, and NRZ data.)

The RDPLS signal is actually digitized MFM data, so it needs to be converted to NRZ data and to be sent to the Controller PCB.

It is also used to detect Sector Marks.

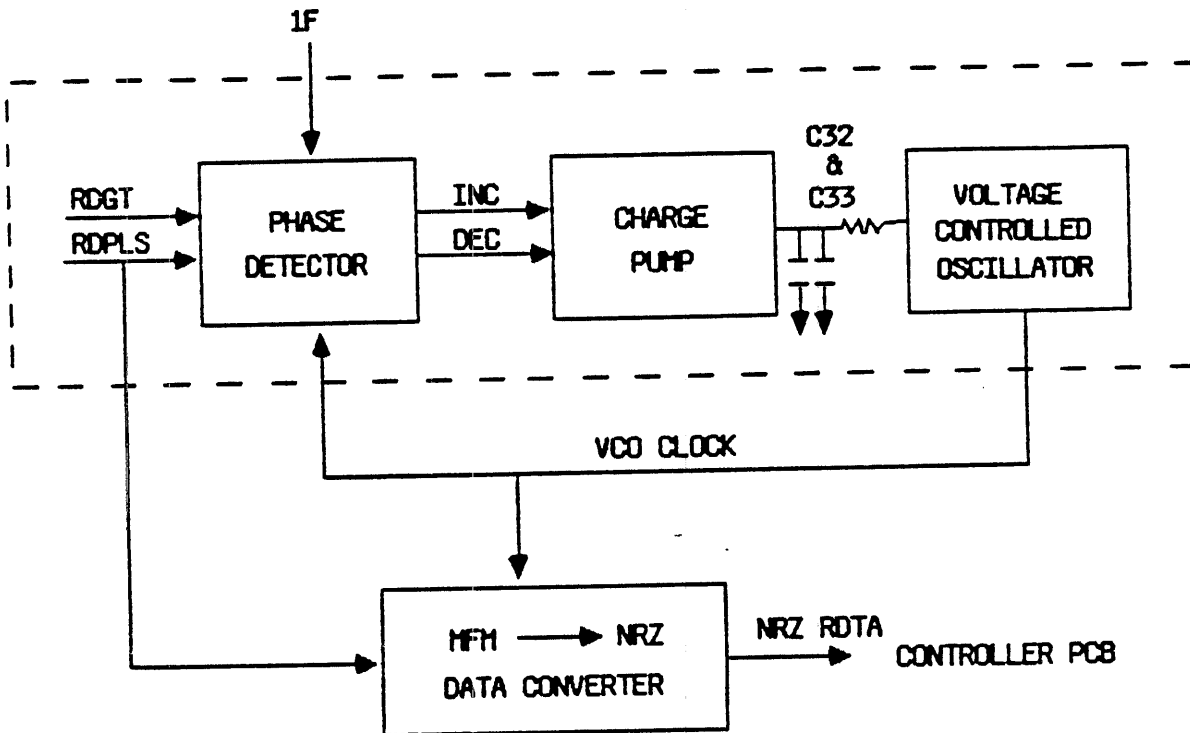
The output of pins 12 and 13 are sent down to the Sector Mark Detector. The RDPLS is gated down through transistors on U12, which pump a charge to C23 at the input of U13.

If there are no read pulses for approximately 10 ms (this can only happen during a sector mark), R71 slowly discharges C23 and causes U13 pin 12 to go high.

This signal is integrated to pin 7 of U13, which produces a 2 us pulse, called SECTOR, to the Z8 on the Controller PCB to notify it that a sector mark has occurred.

When read pulses reappear (as in the sync field at the beginning of a sector), C23 quickly recharges and U13 pin 12 goes low again.

# PHASE LOCK LOOP



### 4.3 PLL (Phase Locked Loop)

All of the circuitry described prior to this point is constantly enabled.

However, from this point on, signals will be allowed to pass only when enabled by the RDGT signal from the Z8 on the Controller.

The block diagram on the opposite page shows the PLL (Phase Locked Loop) on the Analog PCB.

The PLL provides a clock frequency in sync with the incoming MFM digitized data signal to enable the MFM to NRZ Data Converter to perform its function and to forward the serial NRZ data stream to the Controller PCB.

(for information on Modified Frequency Modulation refer to the MFM explanation at the end of this discussion).

The PLL has two modes:

1. The PLL is put in the Idle mode when the RDGT signal from the Z8 on the Controller PCB is inactive (any time the Z8 is not actually performing a Read operation; i.e., Write or Idle).

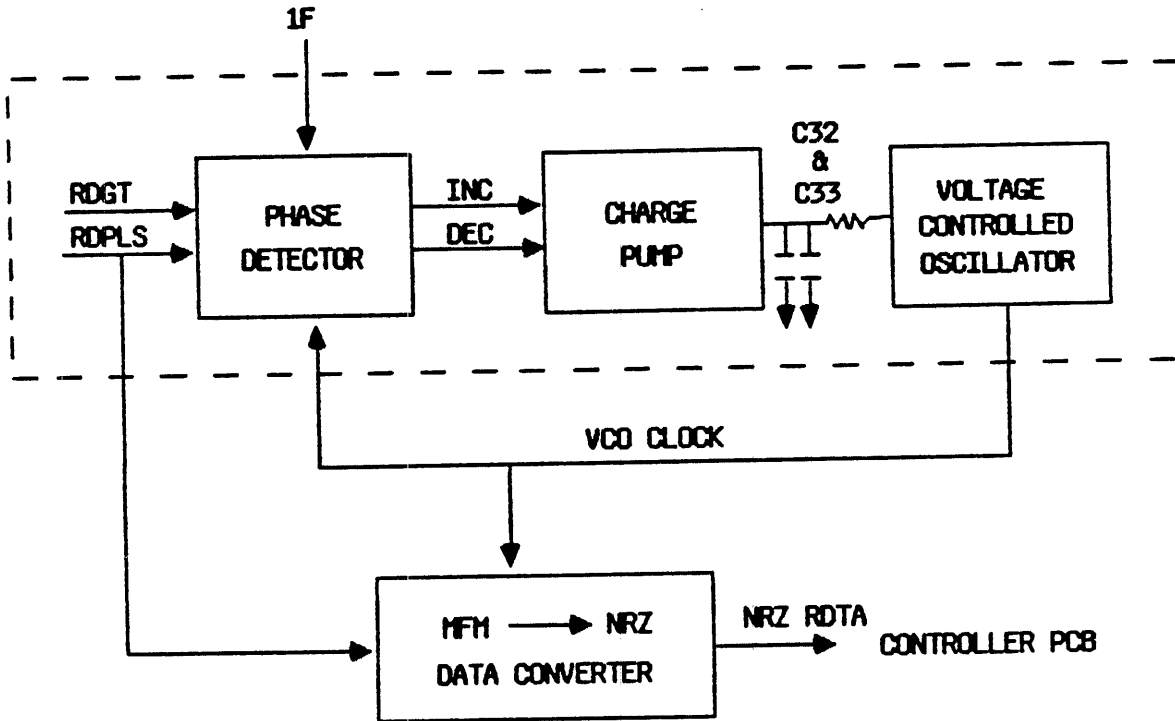
During the Idle mode the PLL syncs the VCO to the master clock frequency from the Controller PCB. This mode has no real purpose and so will not be discussed any further.

2. The PLL is put in the Read mode when the Z8 makes RDGT active during a Read operation. During the Read mode, the PLL syncs the VCO to the incoming MFM digitized data signal. This is performed as follows.

The Phase Detector compares the phase of the VCO clock frequency with the digitized data pulses (RDPLS) from the read analog signal.

If the Phase Detector receives a RDPLS before it receives a VCO pulse, then the VCO's phase is lagging behind the incoming data, and it needs to speed up. So, the Phase Detector generates the INC (increase) signal to the Charge Pump circuit.

## PHASE LOCK LOOP





#### 4.3 PLL (Phase Lock Loop) (continued)

The Charge Pump circuit is then enabled to put a positive charge on C32 and C33.

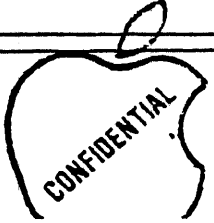
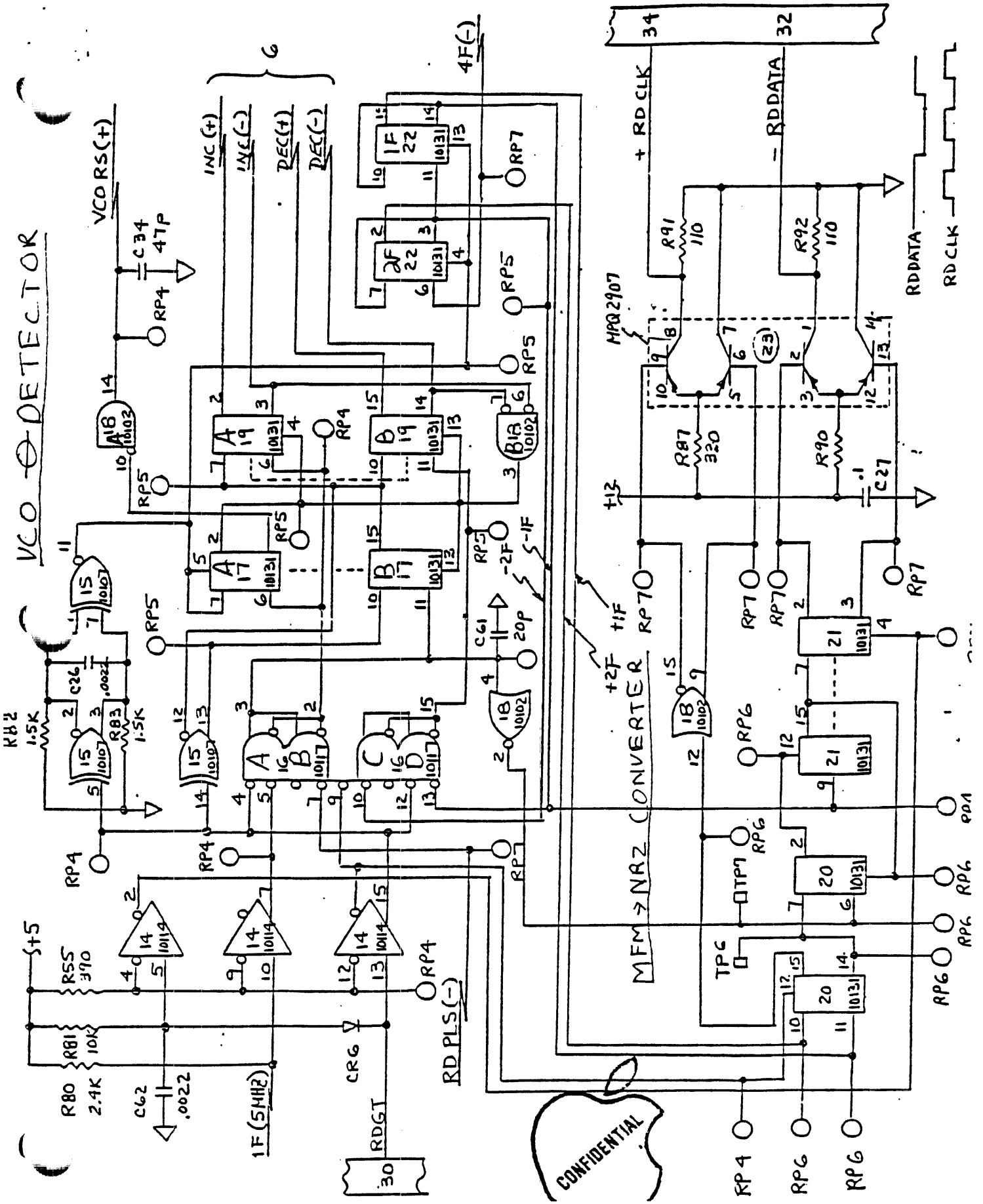
C32 and C33 store the VCO control voltage level that controls the frequency produced by the VCO. The more positive input to the VCO now causes it to increase its output frequency to catch up to the frequency of the incoming data.

If the Phase Detector receives a VCO pulse first (before a RDPLS), then the VCO's phase is leading that of the incoming data, and it needs to slow down.

So, the Phase Detector generates the DEC (decrease) signal to the Charge Pump circuit. The Charge Pump circuit is then enabled to put a negative charge on C32 and C33.

The more negative input to the VCO now causes it to decrease its output frequency, to try to slow down to the frequency of the incoming data.

The different circuits in the PLL are explained in greater detail on the following pages.



## Analog PCB Circuit Descriptions

### 4.3.1 VCO Phase Detector and MFM to NRZ Data Converter Circuits

There are two main circuits shown on the opposite page, the VCO Phase Detector (U15, 16, 17, 18, 19, and 22) and the NRZ to MFM converter (U20 and 21).

The VCO Phase Comparator compares the phase of the clocks from the VCO (Voltage Controlled Oscillator) with those of the incoming analog read signal.

The 20 MHz (4F) output of the VCO comes in to pin 6 of FF "A" on U22. FF "A" of U22 divides 4F to 2F (10 MHz), FF "B" divides 2F into 1F (5 MHz).

Pins 2, 14, and 15 from U22 go to the MFM to NRZ data converter. Pin 3 goes to Selector Gate "C" on U16.

The Selector Gates are the inputs to the Phase Detector and are actually four separate Nand gates.

#### VCO Phase Detector Idle Mode

During Idle mode, RDGT from the Z8 through pin 15 of U14 is low. This enables Selector Gate "A" to pass the 1F master clock frequency and Selector Gate "D" to pass the 1F VCO frequency.

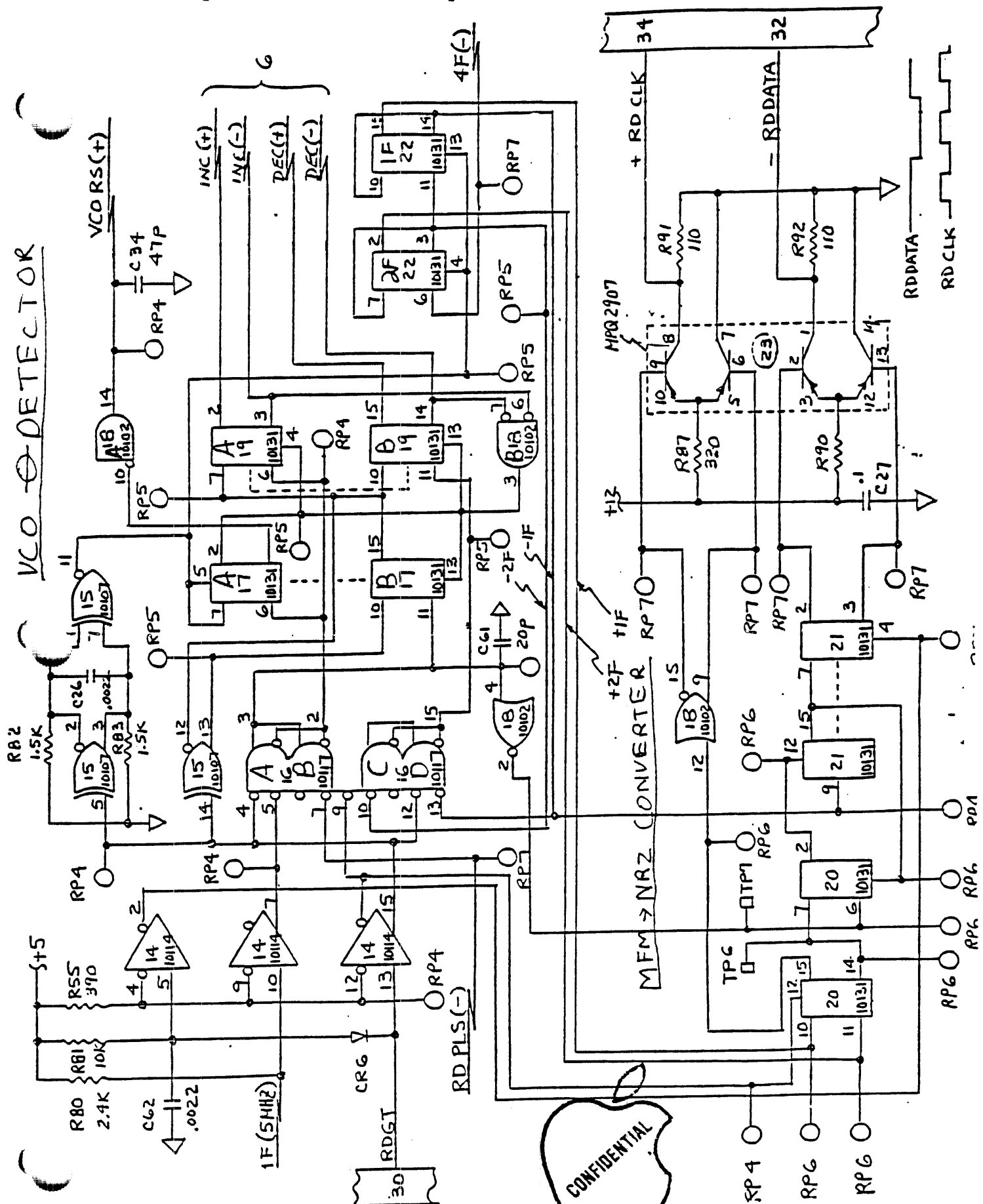
This keeps the VCO in sync with the master clock on the Controller PCB (there is no real reason for this, because the output NRZRDTA is not enabled to go to the Controller PCB.).

#### VCO Phase Detector Read Mode

When the Z8 is performing a Read operation, RDGT is high, enabling Selector Gate "B" to pass RDPLS (digitized MFM read data) and Selector Gate "C" to pass the 2F VCO frequency. (Pin 9 is actually common to both Selector Gates "B" and "C".)

When the Z8 first initiates the Read mode by setting the RDGT signal high, RDGT enters pin 5 of U15 to generate a reset signal to flipflops "A" and "B" in U19 and flipflop "B" in U17.

The reset signal from pin 11 of U15 also presets flipflop "A" in U17 causing the VCRS (VCO Reset) signal out of gate "A" of U18. (Incidentally it resets the VCO as its name implies.)



VCO DETECTOR

CONFIDENTIAL

## Analog PCB Circuit Descriptions

If the Phase Detector receives a RDPLS before it receives a VCO pulse, then that means the VCO's phase is lagging behind the incoming data so the VCO needs to speed up.

In this case the low out of pin 2 of Selector Gate "B" caused by the RDPLS sets FF "A" in U19 through pin 6, causing it to generate the INC (increase) signal to the Charge Pump circuit.

This signal enables the Charge Pump to put a positive charge on C32, and C33 causing the VCO to speed up.

Later, when the 2F signal from the VCO causes Selector Gate "C" to output a low, it will set FF "B" in U19 through pin 11, gate "B" in U18 will then be fully enabled to reset the FFs U17, and 19.

If the Phase Detector receives a VCO pulse first before a RDPLS, then that means the VCO's phase is leading that of the incoming data so it needs to slow down.

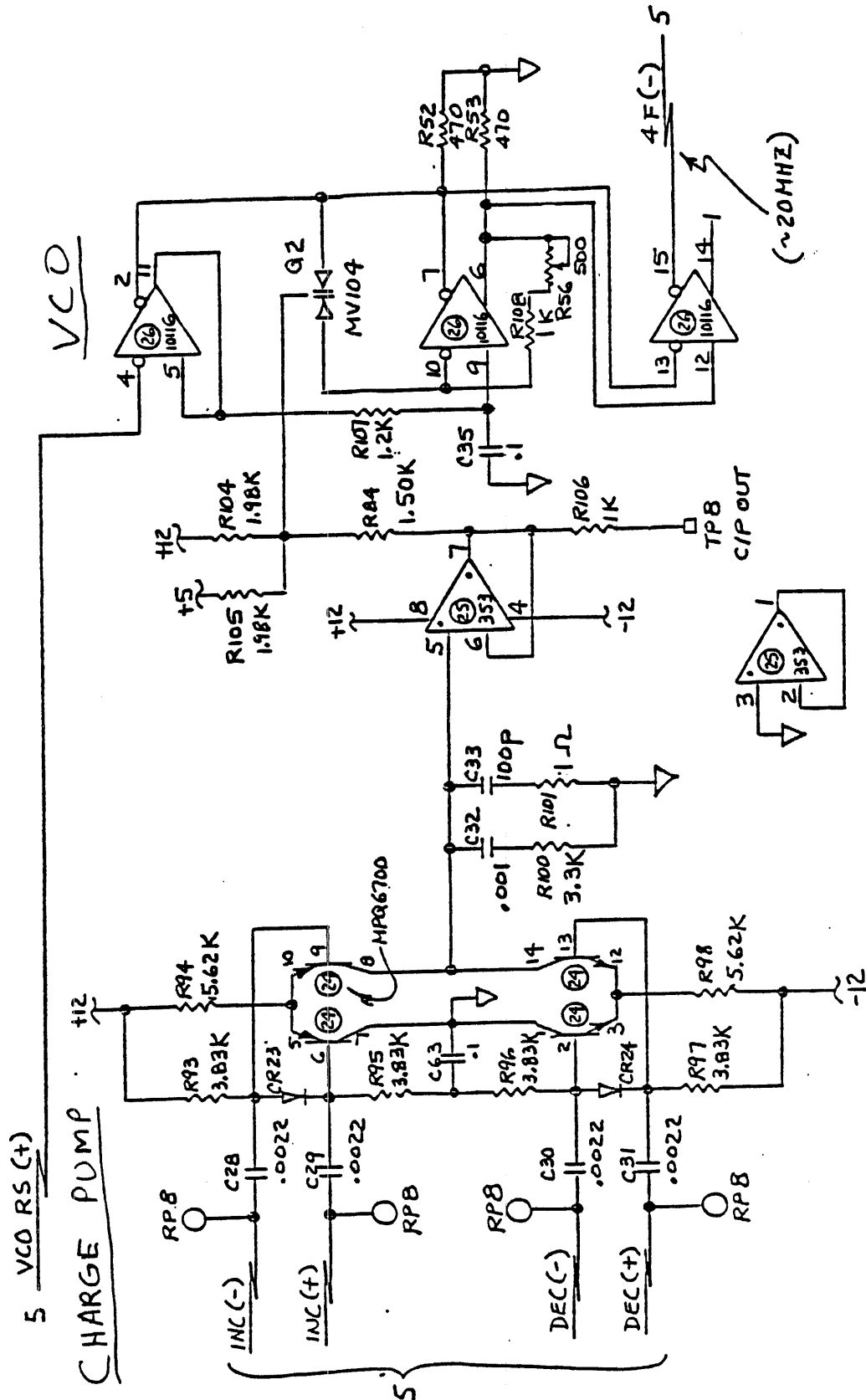
In this case the low out of pin 15 of Selector Gate "C" caused by the VCO 2F signal sets FF "B" in U19 through pin 11 causing it to generate the DEC (decrease) signal to the Charge Pump circuit.

This signal enables the Charge Pump to put a negative charge on C32, and C33 causing the VCO to slow down.

Later when the RDPLS signal arrives, it will cause Selector Gate "B" to output a low, setting FF "A" in U19 through pin 6, gate "B" in U18 will then be fully enabled to reset the FFs U17, and 19.

The RDPLS's are gated down to U20, which takes the digitized MFM data stream and beats it against the function of 1F and 2F ((VCO) now in sync with the incoming data) to convert it to NRZ data.

The results, RD CLK and RD DATA (this data is in NRZ form) are sent to the Controller PCB.



### 4.3.2 Charge Pump and VCO circuits

There are two circuits shown on the opposite page, the Charge Pump on the left and the VCO on the right.

If the Phase Detector receives a RDPLS before it receives a VCO pulse, the VCO's phase is lagging behind the incoming data, so the VCO needs to speed up.

In this case, a high INC + (increase) and a low INC - signal come from the Phase Detector. The low INC - turns its NPN transistor on to send a negative voltage to C32 and C33.

U25 amplifies the negative charge on C32 and C33 to Q2 in the VCO. Q2 is biased by the charge on C32 and C33 to control the frequency produced by the VCO.

If the Phase Detector receives a VCO pulse before it receives a RDPLS then the VCO's phase is leading the incoming data, so the VCO needs to slow down.

In this case, a high DEC + (decrease) and a low DEC - signal come from the Phase Detector.

The high DEC + turns its PNP transistor on to send a positive voltage to pin 5 of an amplifier in U25. Which puts the positive charge on to C32 and C33 for storage, etc.

WHAT IS MFM (Modified Frequency Modulation) ?:

MFM is a scheme in which the ones and zeros of a digital bit stream are converted to a stream of transitions (phase reversals) according to the following rules:

1. Ones always cause a pulse at center cell time.
2. No more than two cells can occur without a transition.
3. Only one transition can occur per cell time.
4. Zeros will cause a pulse at the start cell boundary, if not preceded by a one.

Look at a bit stream of 001011000.

cell time	!	.....	!	.....	!	.....	!	.....	!	.....	!	.....	!	.....	!	.....	!	.....	!
digibits		0		0		1		0		1		1		0		0		0	
pulses		.....	^	.....	.....	^	.....	.....	.....	^	.....	.....	.....	^	.....	.....	.....	.....	.....

Pulses occurred at the start cell times for the first two zeros. Then a pulse occurred at center cell time for the first one.

However, the pulse for the third zero had to be dropped because the following one would have caused another transition to occur less than one cell time away. This would have broken Rule three.

The second and third pulses occur at center cell. (All ones cause pulses at center cell, it's the zeros that get played with.)

The pulse for the fourth zero gets dropped because it was preceded by a one. The fifth and sixth zeros cause pulses at start cell boundaries because no ones interfere.

The diagram on the following page might help you to gain a better understanding of MFM data and its relation to the other methods of modulating data that are used in the Pro-File.

For the Pro-File, the data frequency is 5 MHz, sometimes referred to as 1F (2F would be 10 MHz, 3F would be 15 MHz, etc.).



WHAT IS PRECOMPENSATION ?

When one records things at high density on magnetic media, a phenomenon occurs, called, "don't get too close or I'll push you away." This refers to the polarity of the small magnetic fields, on the disk surface associated with each write pulse.

Example:

```
pulses .....
time   ! 1 ! 1.5 ! 2.0 ! 1 ! 1.5 ! 1 !
push   <- -> -> -> <- -> <- ->
direction
```

Once data is laid down on the disk, the fields associated with each pulse tend to bend away from their neighbors.

If the data were to be written with no procompensation, three conditions could occur when the data are read back from the disk.

1. **Early** - a bit would be picked up too soon in relation to the last bit read.
2. **Late** - a bit would be picked up too late in relation to the last bit read.
3. **On time** - if no pushaways occur, the data bits will be picked up right where they should be, according to MFM rules.

To counteract the bit shifting in condition one or two, when the NRZ to MFM Write Encoder and Data Precompensator converts NRZ data to MFM data, it also examines the relationship between each bit in the data stream and its immediate neighbors to determine if it is a one followed by a one, a zero followed by a one, and so forth.

The Data Precompensator uses this information to determine if the pushaway phenomenon would occur between the bits in that pair.

The Precompensator can shift the actual pulse timing for Write data in one direction or the other in 15 ns increments.

## Precompensation: (continued)

This slight compensation makes the pulses read back during the Read operation appear to be occurring at the correct time.

If a bit pair looks like pushaway might cause a bit to be read early, the Precompensator will direct that bit to be written that much later.

If a pair looks like pushaway would cause a bit to be read late, the Precompensator will direct that bit to be written that much earlier.

And if the bit pair looks like no pushaway will occur, the Precompensator will allow it to be written as is.

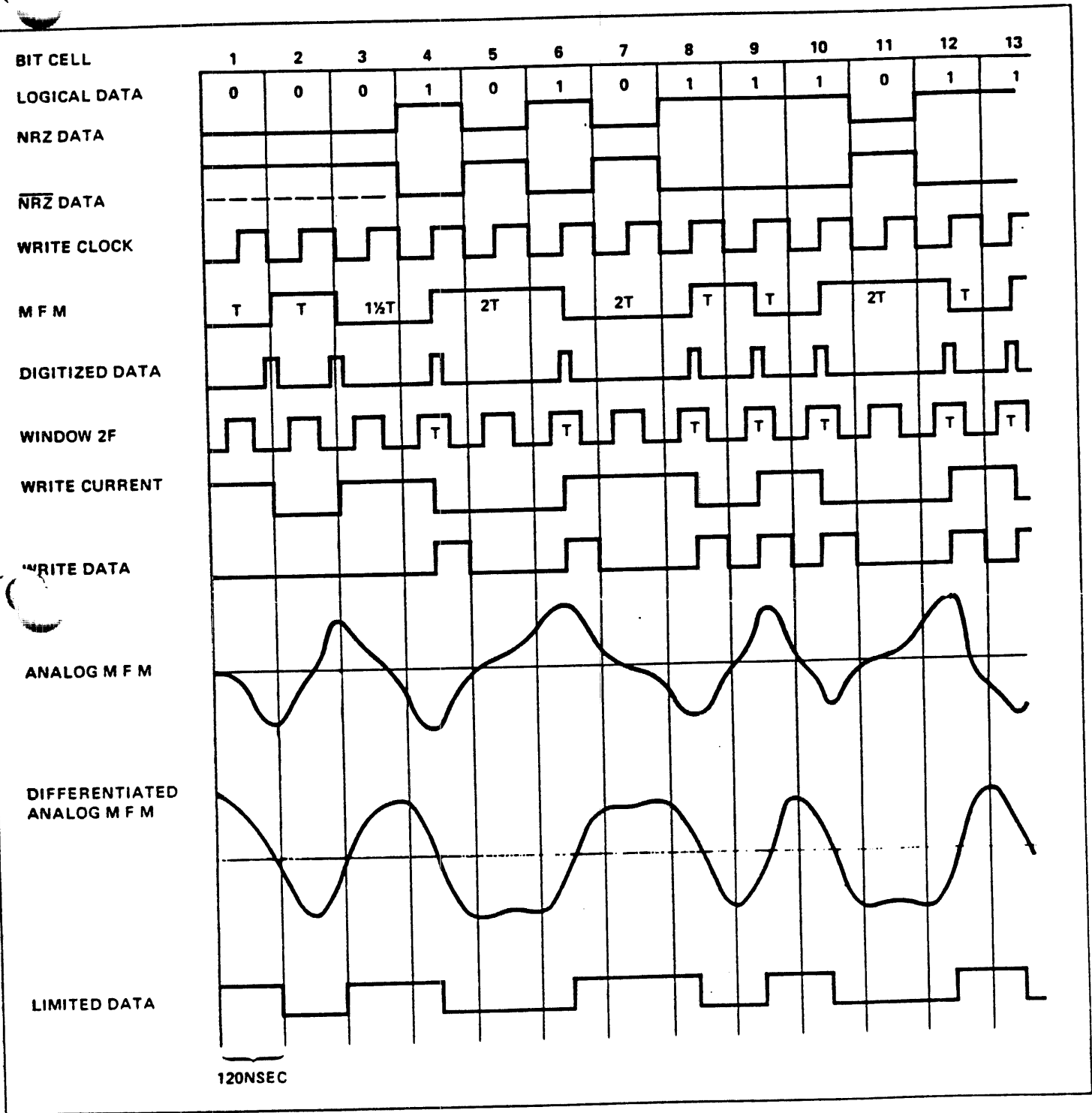
Again, for clarity, if the pushaway effect was not compensated for, the data bits, when they were read, would be time shifted, causing read data errors.

The Write Precompensator identifies the shift that would occur and compensates for it by shifting the write timing the opposite direction of the shift.

That is if a bit would have the tendency to come early it would be retarded. If a bit would have the tendency to come late, it would be advanced. If it was going to be on time, why mess with it.

That's precompensation, and it only occurs on the inside tracks, on the outside tracks the bits are far enough apart that pushaway is not a factor.

# Analog PCB Circuit Descriptions



INDEXED L S O F M A T E R I A L

PROFILE CONTROLLER CARD SVCE STOCK

UMI EA

ABCI \*

PR S T S A P

CD C Y P B L U M

EXTENDED

QTY PER

UM

QTY PER

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QTY PER

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QTY PER

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COMPONENT PART NUMBER

ITEM LEVEL

002 2

005 2

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003 2

008 2

002 3

001 3

000 4

063 4

030 4

016 4

036 4

040 4

042 4

037 4

075 4

039 4

041 4

077 4

035 4

034 4

070 4

001 4

043 4

045 4

032 4

029 4

009 4

026 4

025 4

017 4

027 4

019 4

014 4

020 4

003 4

002 4

030 4

015 4

047 4

024 4

011 4

008 4

073 4

071 4

072 4

012 4

A NOT USED THIS ASSEMBLY

A NOT USED THIS ASSEMBLY

A SPEC SERVICE PCB ASSY PKG PROCEDU

A TAG, REPAIR AND RETURN-SVC

MC ASSY, PCB TSTD, CONTROLLER

B IC SOCKET MICROPRO, W/24P PIGGYBA

1J ASSY, PCB, UNISTD, CONTROLLER, PROFIL

IC SCHEMATIC, CONTROLLER BD, PROFILE

A RES 1/4W 5K 100 OHM

A RES 1/4W 5K 1K OHM

A RES 1/4W 5K 10K OHM

A RES 1/4W 5K 1.5K OHM

A RES 1/4W 5K 200 OHM

A RES 1/4W 5K 30K OHM

A RES 1/4W 5K 3.3K OHM

A RES 1/4W 5K 33K OHM

A RES 1/4W 5K 3.9K OHMS

A RES 1/4W 5K 51 OHM

A RES 1/4W 5K 5.1K OHM

MA RES ARRAY 7 X 2K

MA RES ARRAY 7 X 10K

B RES. ARRAY, 47 OHM

B RESISTOR ARRAY, 6 X 330 OHMS

A CAP. 47UF 10V AXIAL

18 CAP, CER. AX. .1UF Z5U 25V

A CRYSTAL, 10MHZ

A IC, 7406

A IC, 74LS00N

A IC, 74LS02N

A IC, 74LS08

A IC, 74LS14

A IC, 74LS109

A IC, 74LS153

A IC, 74LS161

A IC, 74LS163

A IC, 74LS174

A IC, 74LS240

A IC, 74LS244

A IC, 74LS257

A IC, 74LS280

A IC, 74LS323

A IC, 74LS377

A IC, 74S74

A IC, 74S86

0 IC, 1024 X 4 STATIC RAM 2114

A PROM, 512 X 8 (UNPROGRAMMED)

A PROG OCT 16 INPT AND-OR-INVT GT A

A PROM, MMI 6309-1

MA PROGRAMMABLE INTERVAL TIMER

ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

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ECN1 3007 ASSEMBLY QTY: 1 DATE: 13-SEP-82

PRINTED 21-MAY-63 0711Z

ACTIVITY DATE: ALL

PARENT PART: 661-92049

INDEXED L6 OF MATERIAL

PROFILE CONTROLLER C.A. SVCE STOCK UMS EA PROD CODE1  
ERCI A SRCE CODE1 TYPE1 ABC1 PLAN CODE1 U

ECN 8007 ASSEM QTY 1  
DATE: 13-SEP-62

ECN CHG DATE START S/N CLOSE S/N  
04-MAY-62  
12-NOV-61  
12-NOV-61  
16-NOV-62

ITEM	LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	PR ST S A P	UMS EA	PROD CODE1	EXTENDED	START	S/N	CLOSE
				CD C Y P B L U M		PLAN CODE1	QTY PER	DATE		DATE
008	4	337-8603	B IC SOCKET MICROPRO. W/2P PIGGYBA	RL P 1	0		0	04-AUG-61		04-MAY-62
010	4	337-9401	A CRC GENERATOR/CHECKER	RL P 1	0		0	31-AUG-61		
021	4	341-0066	A PROM, U29	RL A 1	0		0	13-NOV-61		
022	4	341-0067	A PROM, U37	RL A 1	0		0	13-NOV-61		
007	4	341-0068	A RAMPAL	RL P 1	0		0	13-NOV-61		
031	4	341-0080	B PROG PROM 2K PROFILE CONTROLLER	RL P 1	0		0	13-NOV-61		
074	4	341-0129	A EPROM, 2048 X 8 2716	RL A 1	0		0	13-NOV-61		
001	4	351-2074	6A QUAD DARLINGTON TRANSISTOR ARRAY	RL P 1	0		0	13-NOV-61		
028	4	359-4024	A VOLTAGE CONTROLLED MULTIVIBRATOR	RP P 1	0		0	31-AUG-61		
023	4	371-4001	A DIODE, 1N4001	RP P 1	0		0	31-AUG-61		
033	4	371-4128	A DIODE, ZENER, 60V, 250MW	RP P 1	0		0	13-NOV-61		
064	4	371-4148	A DIODE, 1N4148	RP P 1	0		0	13-NOV-61		
062	4	400-1406	IC SCREW, 4-40 X 3/8 CRS RES PN HD	EX X 7	0		0	31-AUG-61		
055	4	511-1401	C SOCKET, IC 14 PIN	RP P 1	0		0	31-AUG-61		
056	4	511-1601	C SOCKET, IC 16 PIN	RP P 1	0		0	31-AUG-61		
057	4	511-1801	C SOCKET, IC 18 PIN	RP P 1	0		0	31-AUG-61		
058	4	511-2001	C SOCKET, IC 20 PIN	RP P 1	0		0	31-AUG-61		
059	4	511-2401	C SOCKET, IC 24 PIN	RP P 1	0		0	31-AUG-61		
060	4	511-4001	C SOCKET, IC 40 PIN	RP P 1	0		0	31-AUG-61		
061	4	515-0005	B PIN, SINGLE	RP P 1	0		0	31-AUG-61		
054	4	515-0053	MB CONN, STRAIGHT HEADER 2 PIN	RP P 1	0		0	31-AUG-61		
053	4	515-0082	A HEADER, 10 PIN RT. ANGLE W/O EARS	RP P 1	0		0	1031-AUG-61		16-NOV-62
066	4	515-0150	MA HEADER, RT ANGLE 5 PIN .156 CENTE	RP P 1	0		0	1031-NOV-61		
067	4	515-0160	MA HEADER, RT ANGLE 2 PIN .100 CENTE	RP P 1	0		0	1031-NOV-61		
065	4	519-0100	6A CONN, 90 D, PCB MT MET. LNG FTPRINT	RP P 1	0		0	1031-NOV-61		
049	4	520-0011	A PLUG CONT. KEY D SUBMINI CONNECTO	EX X 7	0		0	31-AUG-61		
068	4	571-0001	A WIRE, BUS BAR, 20 AWG, .5 IN.	EX X 7	0		0	31-AUG-61		
046	4	820-0055	E PCB, CONTROLLER, PROFILE	RP P 1	0		0	31-AUG-61		
069	4	835-0150	A NUT/WASHER ASSY, (KEPS) 4-40	EX P 7	0		0	13-NOV-61		
007	2	665-92049	A PROFILE CONTROLLER CARD EXCHANGED	EX X 7	1		1	13-SEP-62		
001	3	664-92049	A PROFILE CONTROLLER CARD DEF FR EX	EX X 7	1		1	13-SEP-62		
001	2	942-0160	A MAILER, ONE PIECE 12 1/2 X 9 1/2 X	EX X 7	1		1	13-SEP-62		
004	2	944-0006	MA FOAM, ESTER 11 X 8 1/2 X 3/4	EX X 7	2		2	13-SEP-62		
006	2	946-0001	C TAPE, SEALING GLASS WEBB 3/4	EX X 7	0.0003		0.0003	13-SEP-62		

INDEXED MATERIAL

ECMI 8007 ASSEMBLY QTY 1  
DATE 13-SEP-82

PROF ANALOG CARD SVCE STOCK  
ERCI A SRCE CODE 1 TYPE 7

UMI EA  
ABC: \*

ACTIVITY DATE: ALL  
PARENT PART: 661-92048

ITEM	LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	PR 8 T S A P	UM	EXTENDED QTY PER	ECM CHG	START DATE	8/N	DATE	8/N	CLOSE
008	2	000-0001	A NOT USED THIS ASSEMBLY	D *	D U EA	0	NONE	13-SEP-82				
000	2	070-0004	A SPEC SERVICE PCB ASSY PKG PROCEDU	D *	* U EA	0	800713	SEP-82				
003	2	073-0002	A TAG, REPAIR AND RETURN-SVC	D *	* U EA	1	800713	SEP-82				
008	2	656-4101	A ASSY, PCB TSTD, ANALOG	MT A 1	* P EA	0	P11113	SEP-82				
001	3	656-0101	1H ASSY, PCB UNTSTD, ANALOG, PROFILE	MU A 1	* P EA	0	P48931	AUG-81				
000	4	050-5005	IC SCHEMATIC, ANALOG BD, PROFILE	D D 7	* U EA	0	P41801	MAR-82				
050	4	101-4010	A RES 1/4W 5K 1 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
051	4	101-4101	A RES 1/4W 5K 100 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
053	4	101-4102	A RES 1/4W 5K 1K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
068	4	101-4103	A RES 1/4W 5K 10K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
083	4	101-4104	A RES 1/4W 5K 100K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
080	4	101-4111	A RES 1/4W 5K 110 OHM	RP P 1	S C P EA	0	757	28-JUL-81				
064	4	101-4121	A RES 1/4W 5K 120 OHMS	RP P 1	S C P EA	0	426	28-JUL-81				
077	4	101-4122	A RES 1/4W 5K 1.2K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
075	4	101-4123	A RES 1/4W 5K 12K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
072	4	101-4151	A RES 1/4W 5K 150 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
061	4	101-4152	A RES 1/4W 5K 1.5K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
056	4	101-4182	A RES 1/4W 5K 1.8K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
081	4	101-4201	A RES 1/4W 5K 200 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
069	4	101-4203	A RES 1/4W 5K 20K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
062	4	101-4220	A RES, 1/4W 22 OHM	RP P 1	S C P EA	0	620	28-JUL-81				
055	4	101-4241	A RES 1/4W 5K 240 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
079	4	101-4242	A RES 1/4W 5K 2.4K OHM	RP P 1	S C P EA	0	757	28-JUL-81				
067	4	101-4243	A RES 1/4W 5K 24K OHMS	RP P 1	S C P EA	0	426	28-JUL-81				
066	4	101-4244	A RES, 1/4W 5K 240K OHM	RP P 1	S C P EA	0	626	28-JUL-81				
078	4	101-4272	A RES, 1/4W 5K 2.7K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
082	4	101-4301	A RES, 1/4W 5K 300 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
070	4	101-4331	A RES 1/4W 5K 330 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
073	4	101-4332	A RES 1/4W 5K 3.3K OHM	RP P 1	S C P EA	0	620	28-JUL-81				
089	4	101-4390	A RES 1/4W 5K 39 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
058	4	101-4391	A RES 1/4W 5K 390 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
060	4	101-4392	A RES 1/4W 5K 3.9K OHMS	RP P 1	S C P EA	0	426	13-APR-83				
052	4	101-4471	A RES 1/4W 5K 470 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
084	4	101-4473	A RES 1/4W 5K 47K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
065	4	101-4511	A RES 1/4W 5K 510 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
071	4	101-4561	A RES 1/4W 5K 560 OHM	RP P 1	S C P EA	0	426	28-JUL-81				
085	4	101-4681	A RES 1/4W 5K 680 OHMS	RP P 1	S C P EA	0	426	28-JUL-81				
074	4	101-4751	A RES 1/4W 5K 750 OHM	RP P 1	S C P EA	0	757	28-JUL-81				
063	4	101-4752	A RES 1/4W 5K 7.5K OHM	RP P 1	S C P EA	0	426	28-JUL-81				
076	4	101-4822	A RES, CARBON FILM 8.2K OHM	RP P 1	S C P EA	0	C12726	JUL-81				
057	4	101-4823	A RES, 1/4W 5K 82K OHM	RP P 1	S C P EA	0	757	28-JUL-81				
048	4	108-1543	A RES, 1/8W 1K 1.54K OHM 200PPM	RP P 1	S C P EA	0	768	28-JUL-81				
082	4	108-1783	A RES, 1/8W 1K 1.78K OHM 200PPM	RP P 1	S C P EA	0	768	28-JUL-81				
091	4	108-1963	A RES, 1/8W 1K 1.96K OHM	RP P 1	S C P EA	0	DC4901	MAR-82				
047	4	108-3833	A RESISTOR, 3.83K OHM	RP P 1	S C P EA	0	DC4931	JUL-81				
039	4	108-3923	A RES, 3.92K OHM 1%	RP P 1	S C P EA	0	605	28-JUL-81				
046	4	108-4531	A RES, 1/8W 1K 45.3 OHM, 200PPM	RP P 1	S C P EA	0	768	28-JUL-81				
043	4	108-5623	A RES, 1/8W 1K 5.62K OHM 200PPM	RP P 1	S C P EA	0	768	28-JUL-81				
080	4	109-0005	A POT, TRIM 500 OHM, 20K	RP P 1	S C P EA	0	C04518	MAY-82				
098	4	109-0910	A POT, 500 OHM 18 TURN	RP P 1	S C P EA	0	808	28-JUL-81				

02-MAR-82

ACTIVITY DATES ALL

PARENT PARTS 661-92048

INDEXED LB OF MATERIAL

PROFILE ANALOG CARD STOCK  
ERC1 A SRCE CODES TYPE1 7

UMI EA  
ABCI \*

PROD CODES  
PLAN CODES U

ECNI 8007 ASSEMBL QTYI 1  
DATEI 13-SEP-82

ITEM	LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	PR	S	T	S	A	P	EXTENDED	ECN	START	CLOSE
				CD	C	Y	P	B	L	UM	CHG	DATE	S/N
099	4	109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS	RP	P	1				C P EA	0	10510-MAY-82	
038	4	111-0023	A RESISTOR ARRAY, 7 X 560 OHMS	RP	P	1				C P EA	0	792 28-JUL-81	
094	4	111-0024	A RESISTOR ARRAY, 7 X 4.7K OHMS	RP	P	1				C P EA	0	792 28-JUL-81	
059	4	127-0100	B CAP, 4.7UF 20% 10V AXIAL	RP	P	1				* P EA	0	C18928-JUL-81	
037	4	127-0101	B CAP, 10UF 20% 15/16V AXIAL	RP	P	1				* P EA	0	C18928-JUL-81	
029	4	130-0002	18 CAP, .01UF +80/-20% Z5U 25V	RP	P	1				C P EA	0	C23228-JUL-81	
097	4	130-0003	18 CAP, .01UF +80/-20% Z5U 25V	RP	P	1				C P EA	0	C232	
028	4	130-0007	18 CAP, CER. AX. .1UF Z5U 25V	RP	P	1				C P EA	0	C23201-MAR-82	
031	4	130-0200	A CAP, .001UF 10%(K) AXIAL	RP	P	1				C P EA	0	768 28-JUL-81	
030	4	130-0201	A CAP, .0022UF 10% AXIAL	RP	P	1				C P EA	0	768 28-JUL-81	
036	4	137-5401	A CAP, 20PF, 5% 500VDC	RP	P	1				C P EA	0	741 28-JUL-81	
035	4	137-5701	0 CAP, 47PF 5% 200PPM 500VDC	RP	P	1				C P EA	0	442 28-JUL-81	
034	4	137-5901	A CAP, 100PF 5% 200PPM 500VDC	RP	P	1				C P EA	0	442 28-JUL-81	
032	4	137-6101	0 CAP, 150PF 5% 200VDC	RP	P	1				C P EA	0	741 28-JUL-81	
033	4	137-6301	A CAP, 150PF 5% 200VDC	RP	P	1				C P EA	0	757 28-JUL-81	
027	4	151-4701	A CHOKE, 5.6UH, 10% AXIAL	RP	P	1				* P EA	0	792 28-JUL-81	
021	4	156-0100	A DELAY LINE 14 PIN DIP 100 OHM, 50	RP	P	1				* P EA	0	792 28-JUL-81	
022	4	156-0110	A DELAY LINE 14 PIN DIP 500 OHM 100	RI	P	1				C P EA	0	C06328-JUL-81	
007	4	301-0045	A IC, 7445	RI	P	1				C P EA	0	C06328-JUL-81	
001	4	301-0074	A IC, 7474	RI	P	1				C P EA	0	442 28-JUL-81	
005	4	305-0014	A IC, 74LS14	RI	P	1				C P EA	0	442 28-JUL-81	
002	4	305-0174	A IC, 74LS14	RI	P	1				C P EA	0	C06328-JUL-81	
004	4	307-0064	A IC, 74S64	RI	P	1				C P EA	0	741 28-JUL-81	
013	4	325-0102	A QUAD 2-INPUT NOR GATE	RI	P	1				C P EA	0	741 28-JUL-81	
010	4	325-0107	A TRIPLE 2-INPUT EXCL OR/EXCL NOR GA	RI	P	1				C P EA	0	741 28-JUL-81	
008	4	325-0114	A TRIPLE LINE RECEIVER	RI	P	1				C P EA	0	741 28-JUL-81	
009	4	325-0116	A TRIPLE LINE RECEIVER	RI	P	1				C P EA	0	741 28-JUL-81	
012	4	325-0117	A DL 2-AND 2-3-INPT OR-AND/OR-AND-I	RI	P	1				C P EA	0	C25228-JUL-81	
011	4	325-0131	B IC ECL HIGH SPEED DUAL D FLIP-FLO	RI	P	1				* P EA	0	757 28-JUL-81	
006	4	327-0453	A IC, DUAL PERIPHERAL DRIVES	RI	P	1				* P EA	0	642 28-JUL-81	
096	4	335-0007	A PROG HEX 16 INPT REG AND-OR GT	RL	P	1				* P EA	0	P10501-MAR-82	
003	4	341-0069	A MEMPAL	RL	A	1				* P EA	0	750 28-JUL-81	
014	4	351-2907	A IC TRANS ARRAY QUAD PNP GEN	RP	P	1				C P EA	0	750 28-JUL-81	
016	4	351-3127	A TRANSISTOR/ARRAY NPN HIGH FREQ.	RP	P	1				C P EA	0	750 28-JUL-81	
023	4	351-6700	A IC, TRANS. ARRAY QUAD COMP. PAIRS	RI	P	1				C P EA	0	792 28-JUL-81	
058	4	353-0005	A IC REG. +5V 100MA TO 92, 3 TERMNL	RI	P	1				C P EA	0	750 28-JUL-81	
018	4	353-0319	A IC, HIGH SPEED DUAL COMPARATOR	RI	P	1				C P EA	0	750 28-JUL-81	
017	4	353-0353	A DUAL FET OP AMP/BUFFER	RP	P	1				C P EA	0	750 28-JUL-81	
015	4	353-0592	A IC, VIDEO AMPLIFIER	RP	P	1				C P EA	0	750 28-JUL-81	
024	4	371-4152	A DIODE IN4152, FAST SWITCHING	RP	P	1				C P EA	0	750 28-JUL-81	
026	4	375-0010	A DIODE 1.2V TEMP. COMP REFERENCE	RP	P	1				C P EA	0	750 28-JUL-81	
019	4	375-0012	A DIODE VOLTAGE VARIABLE CAPACITANC	RP	P	1				* P EA	0	C30328-JUL-81	
020	4	376-0016	A FET, N-CHANNEL VOLT CONTRL RESIS.	RP	P	1				* P EA	0	799 28-JUL-81	
090	4	511-0801	C SOCKET, IC 8 PIN	RP	P	1				C P EA	0	799 28-JUL-81	
091	4	511-1401	C SOCKET, IC 14 PIN	RP	P	1				C P EA	0	799 28-JUL-81	
092	4	511-1601	C SOCKET, IC 16 PIN	RP	P	1				C P EA	0	799 28-JUL-81	
093	4	511-2001	C SOCKET, IC 20 PIN	RP	P	1				C P EA	0	C11528-JUL-81	
089	4	515-0005	B PIN, SINGLE	RP	P	1				* P EA	0	808 28-JUL-81	
087	4	515-0120	A HEADER, SINGLE ROW 4 PIN, J <sup>1</sup> CNT	RP	P	1				* P EA	0	C14928-JUL-81	
085	4	515-0130	B HEADER, RT ANG, 16 PIN DOUBLE	RP	P	1				* P EA	0		

14-APR-83

02-MAR-82

14-APR-83  
14-APR-83  
14-APR-83  
02-MAR-82

INDEMENT . L B OF MATERIAL

ACTIVITY DATE: ALL

ECNI 8007 ASSEMBLY QTY: 1  
DATE: 13-SEP-82

PROFILE ANALOG CARD SVCE STOCK  
ERCI A SRCE CODE: \* TYPE: 7

PARENT PART: 661-92048

ITEM	LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	PR ST S A P CD C Y P B L UM	UM	EXTENDED QTY PER	ECN CHG	DATE	START S/N	DATE	CLOSE S/N
088	4	515-0131	B HEADER, RT ANG 34 PIN DOUBLE ROM	RP P 1	C P EA	0	C14901	MAR-82			
086	4	515-0140	MA CONN, RT ANGLE HEADER 5 PIN	RP P 1	* P EA	0	808 26	JUL-81			
095	4	620-0054	AE PCB, ANALOG PROFILE	RP P 1	* P EA	0	P21401	MAR-82			
007	2	665-92048	A PROFILE ANALOG CARD EXCHANGED	* 7	* U EA	1	800713	SEP-82			
001	3	664-92048	A PROFILE ANALOG CARD DEF FR EXC	* 7	* U EA	1	802213	SEP-82			
001	2	942-0159	A RETT MAILER, 228.60 X 152.40 X 25.	EX P 7	* P EA	1	800713	SEP-82			
002	2	942-0167	A BAG, BUHL, ANTI-STAT 177.80 X 215.9	EX P 7	* P EA	1	800713	SEP-82			
005	2	948-0019	1A WHITE STYROFOAM FLO-PAK	EX X 7	P B P BG	0.0025	A39313	SEP-82			
006	2	946-0001	C TAPE, SEALING GLASS WEB# 341	EX X 7	P B P RL	0.0003	474 13	SEP-82			



INDEXED MATERIAL

ACTIVITY DATE: ALL

ECMI 8007 ASSEMBLY QTY: 1  
DATE: 13-SEP-62

PROF INTERF CARD SVCE STOCK  
EPC: A SRC CODE: TYPE: 7

UMI EA  
ABC: \*

PROD CODES  
PLAN CODE: U

ITEM	LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	PR	S	T	S	A	P	EXTENDED	START	DATE	8/N	CLOSE	8/N
				CD	C	Y	P	B	L	UM	QTY	PER			
004	2	000-0001	A NOT USED THIS ASSEMBLY	D	*	D	U	E	A	0					
000	2	070-0004	A SPEC SERVICE PCB ASSY PKG PROCEDU	D	*	U	E	A		0					
003	2	073-0002	A TAG REPAIR AND RETURN-SVC	D	*	U	E	A		1					
008	2	656-4103	A ASSY, PCB T870, I/O PROFILE A3	MT	A	1				0					
001	3	656-0103	AD ASSY, PCB UNTSTD, I/O PROFILE, A3	WU	A	1				0					
000	4	050-5007	AA SCHEMATIC, I/O CARD, PROFILE	D	D	7				0					
015	4	101-4103	A RES 1/4W 5K 10K OHM	RP	P	1	P	C	P	E	0				
014	4	101-4332	A RES 1/4W 5K 3.3K OHM	RP	P	1	P	C	P	E	0				
029	4	101-4751	A RES 1/4W 5K 750 OHM	RP	P	1	P	C	P	E	0				
034	4	112-0102	B RES. ARRAY, 47 OHM	RP	P	1	P	C	P	E	0				
021	4	112-0104	B RESISTOR ARRAY, 7 X 470 OHMS	RP	P	1				0				12-NOV-61	
013	4	112-0105	B RESISTOR ARRAY, 8 X 330 OHMS	RP	P	1				0					
035	4	130-0003	1B CAP, .1UF +80/-20% Z5U 25V	RP	P	1	P	C	P	E	0				
016	4	130-0007	1B CAP, CER. AX. .1UF 25U 25V	RP	P	1	P	C	P	E	0				
032	4	132-6101	A BEAD, FERRITE	RP	P	1	P	C	P	E	0				
031	4	159-0009	A IC, 7438	RI	P	1	P	C	P	E	0				
003	4	301-0038	A IC, 74259	RI	P	1	P	C	P	E	0				
028	4	301-0259	A IC, 9334	RI	P	1	P	C	P	E	0				
007	4	301-9334	A IC, 74LS10	RI	P	1	P	C	P	E	0				
004	4	305-0010	A IC, 74LS14	RI	P	1	P	C	P	E	0				
002	4	305-0014	A IC, 74LS16	RI	P	1	P	C	P	E	0				
033	4	305-0038	A IC, 74LS38 QUAD 2 INPUT BUFFER	RI	P	1	P	C	P	E	0				
012	4	305-0109	A IC, 74LS109	RI	P	1	P	C	P	E	0				
005	4	305-0125	A IC, 74LS125	RI	P	1	P	C	P	E	0				
001	4	305-0132	A IC, 74LS132	RI	P	1	P	C	P	E	0				
006	4	305-0138	A IC, 74LS138	RI	P	1	P	C	P	E	0				
009	4	305-0244	A IC, 74LS244	RI	P	1	P	C	P	E	0				
010	4	305-0280	A IC, 74LS280 9-BIT PARITY	RI	P	1	P	C	P	E	0				
011	4	305-0368	A IC, 74LS368	RI	P	1	P	C	P	E	0				
008	4	305-0374	A IC, 74LS374	RI	P	1	P	C	P	E	0				
026	4	400-1406	IC SCREM, 4-40 X 3/8 CRS RES PN HD	EX	X	7	P	C	P	E	0				
022	4	511-1401	C SOCKET, IC 14 PIN	RP	P	1	P	C	P	E	0				
023	4	511-1601	C SOCKET, IC 16 PIN	RP	P	1	P	C	P	E	0				
024	4	511-2001	C SOCKET, IC 20 PIN	RP	P	1	P	C	P	E	0				
025	4	515-0005	B PIN, SINGLE	RP	P	1	P	C	P	E	0				
030	4	519-0100	6A CONN, 90 D, PCB MT MET, LNG FTPRINT	RP	P	1				0					
018	4	520-0011	A PLUG CONT. KEY D SUBMINI CONNECTO	RP	P	1				0					
020	4	620-0056	AC PCB I/O, PROFILE, FOR A3	RM	P	1				0					
027	4	635-0150	A NUT/WASHER ASSY, (KEPS) 4-40	EX	X	7				0					
001	3	665-92050	A PROFILE INTERFACE CARD EXCHANGED	EX	X	7				1					
007	2	664-92050	A PROFILE INTERFACE CARD DEF FR EXC	EX	X	7				1					
002	2	942-0115	A BAG, BUBBLE 8 X 6	EX	X	7				1					
001	2	942-0159	A RETT MAILER, 228.60 X 152.40 X 25.	EX	X	7				1					
003	2	948-0019	1A WHITE STYROFOAM FLO-PAK	EX	X	7				1					
006	2	946-0001	C TAPE, SEALING GLASS WEBM 341	EX	X	7				0.0025					
										0.0003					

EFFICIENT DATE: 09/18/84

PARENT PART: 49K0065

1 LG, PROFILE, "GENERIC" DRIVE - USA UM: EA PROD CODE: DH FCH: F354 ASSEMBLY UTT: 1  
SRC: A SRCO CODE: 0 TYPE: 1 ABC: # PLAN CODE: P DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	QTY	UOM	EXTENDED QTY PER	CHG	DATE	QTY	DATE
001	2	656-8104	1J FG, PROFILE "GENERIC" DRIVE - USA	**	** EA	1	L30515	Mar-83		
003	3	030-0183	1E REGIS. CARD, PERIPH. & SOFTWARE	EX X 7	P C P EA	1	A92715	Mar-83		30-Sep-83
002	3	030-0273	1D UNPACKING INSTRUCTIONS, PROFILE	EX X 7	C P EA	1	F2915	Mar-83		30-Sep-83
001	3	030-0624	1D UNPACKING LIST, PROFILE DISK DRIVE	**	** EA	1	F67515	Mar-83		30-Sep-83
030	3	590-0003	1D CABLE, A.C. POWER CORD	2M P 1	P C P EA	1	AS6230	Jun-83		30-Sep-83
005	3	600-2515	A ASSY, END PAD	MS A 1	** P EA	2	F12515	Mar-83		06-Jul-83
013	3	600-2516	B ASSY, END CAP, PROFILE	MS A 1	** P EA	2	F56815	Mar-83		06-Jul-83
004	3	600-2517	A ASSY., TOP/BOTTOM PAD, PROFILE	**	** EA	2	F26515	Mar-83		06-Jul-83
032	3	602-0041	1E ASSY, SHIPPING CTN - PROFILE FR'S	**	** EA	1	L26707	Jul-83		06-Jul-83
001	4	600-2515	A ASSY, END PAD	MS A 1	** P EA	2	F12507	Jul-83		06-Jul-83
004	4	600-2516	B ASSY, END CAP, PROFILE	MS A 1	** P EA	2	F56807	Jul-83		06-Jul-83
002	4	600-2517	A ASSY., TOP/BOTTOM PAD, PROFILE	**	** EA	2	F26507	Jul-83		06-Jul-83
003	4	942-0117	1C BOX, 29.5 X 21.25 X 16.13, PROFIL	EX X 7	C P EA	1	F39907	Jul-83		06-Jul-83
005	4	942-0142	A BOX, OFF 19.25 X 10.75 X 6.88	EX P 7	** P EA	1	P12507	Jul-83		06-Jul-83
007	4	944-0091	1A CUSHION BLOCK, EPS, PROFILE (TO REFACE ACC KIT)	**	** EA	1	P35407	Jul-83		06-Jul-83
006	4	946-0010	A TAPE, SEALING GLASS WFB #341	EX X 7	B P RL	0.0100	RR3	07-Jul-83		
033	3	656-5105	1C SUB ASSY, PWR CRD KIT, PROFILE	**	** EA	1	L30501	Oct-83		
006	4	030-0183	1E REGIS. CARD, PERIPH. & SOFTWARE	EX X 7	P C P EA	1	A92701	Oct-83		11-Dec-83
002	4	030-0273	1D UNPACKING INSTRUCTIONS, PROFILE	EX X 7	C P EA	1	F72901	Oct-83		
003	4	030-0624	1D UNPACKING LIST, PROFILE DISK DRIVE	**	** EA	1	P67501	Oct-83		
004	4	590-0003	1D CABLE, A.C. POWER CORD	2M P 1	P C P EA	1	A86201	Oct-83		
005	4	942-0017	1D SHRINK WRAP, 12" CENTERFOLDED	EX X 1	P C P RL	1	L30901	Oct-83		
001	4	942-0391	0 TAPE, MASKING PERMACEL #F-786 3/4	EX X 7	P C P EA	1	P56001	Oct-83		
007	4	946-0006	3E INACT.MFG.ASSY, CHASSIS, PROFILE	**	** EA	0	L305	11-Dec-83		
034	3	656-6110	1C SCR 6-32X1/4 FN HD CRS REC STL ZN	EX X 7	C P EA	0	C54014	Dec-82		
008	4	400-1604	1C SCR 6-32X3/8 FN HD CRS REC STL ZN	EX X 1	P C P EA	0	C54001	Jun-83		
008	4	400-1606	1C SCR 6-32X1/2 FN HD CRS REC STL ZN	EX X 7	C P EA	0	C54014	Dec-82		
004	4	400-1608	1C SCR 6-32X3/8 FN HD CRS REC STL ZN	EX X 7	S C U EA	0	C54031	Aug-83		
013	4	403-1606	1C SCR TAP 8-18X.437 FN CRS STL ZN	EX X 7	P C P EA	0	C54014	Dec-82		
009	4	430-1001	1A CONN, D., IDC, 25P, W/O SR	RC P 1	** P EA	0	F60314	Dec-82		14-Apr-83
011	4	590-0046	1B CABLE, FLAT 25 CONDUCTOR	RP P 1	** U EA	0	C78131	Aug-81		
001	5	519-0110	3A REIDENTIFY SEE 560-0203	**	** FT	0	C52301	Oct-83		
002	5	569-0203	A ASSY, PCB TSTD, I/O PROFILE A3	WT A 1	** P EA	0	C52331	Aug-81		30-Sep-83
003	5	590-0052	1F ASSY, PCB UNTSTD, I/O PROFILE, A3	WU A 1	** P EA	0	F11314	Dec-82		14-Apr-83
010	4	656-4103	1R SCHEMATIC, I/O CARD, PROFILE	D D 7	** U EA	0	F78131	Aug-81		
001	5	656-4103	1A RES 10K OHM 1/4W 5%	RP P 1	P C P EA	0	F65104	Jan-82		
000	6	050-5007	R4,5,7				C67531	Jul-81		
015	6	101-4103	R1,3,6				C67531	Jul-81		
014	6	101-4332	R2				C67513	Nov-81		
029	6	101-4751	R2				C67531	Aug-81		12-Nov-81
034	6	112-0102	R1				C67531	Aug-81		
031	5	112-0104	R1				C67531	Aug-81		
013	6	112-0105	R1				C67531	Nov-81		06-Nov-83
036	6	112-0106	R1							

INDENTED FILES OF MATERIAL

PARENT PART: ASH0005  
ECC: A SRCF CODE: G TYPE: 1  
F PART DESCRIPTION: FERRITE  
UM: EA  
PROD CODE: DH  
ECC: F354  
ASSEMBLY QTY: 1  
DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	QTY PER	UNIT	START DATE	END DATE	CLOSE
035	6	1R CAP CER AXIAL .1 UF 480V-20% 25V	0	C P EA	17-May-82		
016	6	1R CAP CER AXIAL .1 UF 480V-20% 25V	0	C P EA			
032	6	1A CAP CER 100 UF 20% 50V	0	C P EA			
031	6	A BEAD, FERRITE	0	C P EA			
003	6	A IC, 7438	0	C P EA			
028	6	A IC, 74259	0	C P EA			
007	6	A IC, 9334	0	C P EA			
004	6	A IC, 74LS10	0	C P EA			
002	6	A IC, 74LS14	0	C P EA			
033	6	A IC, 74LS38 QUAD 2 INPUT BUFFER	0	C P EA			
012	6	A IC, 74LS109	0	C P EA			
005	6	A IC, 74LS125	0	C P EA			
001	6	A IC, 74LS132	0	C P EA			
006	6	A IC, 74LS138	0	C P EA			
009	6	A IC, 74LS244	0	C P EA			
010	6	A IC, 74LS280 9-BIT PARITY	0	C P EA			
011	6	A IC, 74LS368	0	C P EA			
008	6	A IC, 74LS374	0	C P EA			
026	6	1C SCR 4-40X3/8 PM HD GRS RFC STL ZN	0	C P EA			
022	6	C SOCKET, IC 14 PIN	0	C P EA			
023	6	C SOCKET, IC 16 PIN	0	C P EA			
024	6	C SOCKET, IC 20 PIN	0	C P EA			
025	6	1R CONN, PIN, SINGLE	0	C P EA			
030	6	1R CONN, PC 1411, 50 PINS, METAL, INC FTFFI	0	C P EA			
019	6	1R CONN, PIN, 1411, 50 PINS, METAL, INC FTFFI	0	C P EA			
020	6	1R CONN, PIN, 1411, 50 PINS, METAL, INC FTFFI	0	C P EA			
021	6	1R CONN, PIN, 1411, 50 PINS, METAL, INC FTFFI	0	C P EA			

EFFECTIVITY DATE: ALL

PARENT PART: A9M0000

1 FG, PROFILE, 'GENERIC' DRIVE USA UM:EA PRO CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ERC: A SRCO CODE: G TYPE: 1 ARC: \* PLAN CODE: P DATE: 15-Mar-83

INDENTED BILL OF MATERIAL

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	QTY	UOM	EXTENDED QTY PER	CHG	START DATE	END DATE	CLOSE
002	4	3D INACT.MFG SUBASSY,BASE,PROFILE	*	* EA	0	L30514-	Dec-82		
005	5	1C SCR 6-32X1/4 FN HD CRS RFC STL 7N EX X 7	C P EA	0	C54014-	Dec-82			
006	5	1C SCR 6-32X3/8 FN HD CRS RFC STL 7N EX X 1	C P EA	0	C54001-	Apr-83			31-May-83
011	5	1C SCR 6-32X1/2 FN HD CRS REC STL 7N EX X 7	C P EA	0	C54001-	Jun-83			
007	5	1C SCR TAP 4-20X.250 FN CRS RFC STL EX X 7	C P EA	0	C54014-	Dec-82			22-Jun-83
012	5	1C SCR TAP 4-24X.250 FN CRS REC STL	** ** EA	0	C54023-	Jun-83			
001	5	6A SUBASSY COVER,BOTTOM,PROFILE	** ** EA	0	F40801-	Apr-83			
002	6	1A SHIELD,CSA PROFILE	** ** EA	0	F40801-	Apr-83			
001	6	1C COVER, BOTTOM, PROFILE	RM P 1 * P EA	0	F40801-	Apr-83			
002	5	1C SURPANEL, REAR, PROFILE	RP P 1 * P EA	0	F52614-	Dec-82			
008	5	A SUPPORT, PROFILE	RP P 1 * P EA	0	F16814-	Dec-82			
010	5	B COVER, DRIVE, BOTTOM, PROFILE	RM P 1 * P EA	0	F16814-	Dec-82			31-Mar-83
003	5	1A COVER DRIVE, BOTTOM, PROFILE	** ** EA	0	F40801-	Apr-83			
009	5	1C COVER, BOTTOM, PROFILE	RM P 1 * P EA	0	F40814-	Dec-82			31-Mar-83
004	5	MA FOOT, .52HT, SQ	EX X 7 P C P EA	0	545 14-	Dec-82			
005	4	3D INACT.MFG SUBASSY,COVER,PROFILE	** ** EA	0	L30514-	Dec-82			
004	5	1B CARLE, ASSY, LED, PROFILE	RC P 1 * P EA	0	F46414-	Dec-82			
008	6	1A CONN,RCPT,INSUL. DISPL.,2P	RP P 1 * U EA	0	C78131-	Aug-81			
003	6	A TUBING, BRAIDED, 1/8 DIA.	EX X 7 * U IN	0	F10931-	Aug-81			
007	6	1C TUBING, HEAT SHRINK 1/4 ID BLACK	EX X 7 P C P FT	0	C50331-	Aug-81			
006	6	1C TUBING, HEAT SHRINK 1/16 ID BLACK	EX X 7 P C P FT	0	C50331-	Aug-81			
004	6	B WIRE, BLACK 26 AWG, 7 X 34	EX X 7 P * P FT	0	764 31-	Aug-81			
005	6	B WIRE, 26 AWG STRAND, RED	EX X 7 * U FT	0	C01831-	Aug-81			
005	6	MA LED, RED APPLE III DISKABLE	RP X 1 P C P EA	0	552 31-	Aug-81			
001	6	0 GROMET, PANEL MTG. FOR RECT. LAMP	RM X 1 P C P EA	0	442 31-	Aug-81			26-Apr-83
001	6	1B PURCH ASSY,COATD TOP CVR,PRFLE-B	** ** EA	0	L05112-	Dec-83			
001	5	1C COVER, TOP, PROFILE	RM P 1 * P EA	0	P40812-	Dec-83			
001	6	0 GROMET, PANEL MTG. FOR RECT. LAMP	RM X 1 P C P EA	0	442 27-	Apr-83			
008	5	1C COVER, TOP, PROFILE	RM P 1 * P EA	0	F408				11-Dec-83
009	5	1B LABEL, LOGO 16MM BY 16MM	EX X 7 P C P EA	0	F51414-	Dec-82			15-Feb-83
005	5	825-0311	EX X 7 P C P EA	0	F51414-	Dec-82			15-Feb-83
006	5	825-0313	EX P 7 * P EA	0	P51414-	Dec-82			15-Feb-83
007	5	825-0315	EX P 7 * P EA	0	C61114-	Dec-82			
003	5	3A INACTIVE,REIDENTIFIED SEE 830-002	EX X * * P EA	0	C74414-	Dec-82			
002	5	1B NUT, SPEED 'J' TYPE SIZE 8	EX X 7 P C P EA	0	L30514-	Dec-82			
001	4	3A INACT.MFG SUBASSY,HDA/PWR SUP.PROF	** ** EA	0	F26614-	Dec-82			
003	5	A MICROPRCSR-2K PROG ROM FORR PROFI	** ** EA	0	F55814-	Dec-82			
001	5	6C MFG SUBASSY, POWER SUPPLY, PROFIL	** ** EA	0	C54014-	Dec-82			
007	6	1C SCR 6-32X3/16 FN HD CRS REC STL Z	EX P 7 * P EA	0	F26614-	Dec-82			
006	6	MC ASSY, PCB TSTD, CONTROLLER	WT A 1 * P EA	0	C14805-	May-82			14-Oct-82
002	7	B IC SOCKET MICROPRO. W/2AP PIGGYBA	RL P 1 * P EA	0	F65131-	Aug-81			
001	7	1M ASSY,PCB,UNTSID,CONTROLLER,PROFIL	WU A 1 * P EA	0	F65104-	Jan-82			
000	8	1E SCHEMATIC, CONTROLLER RO, PROFILE	D D 7 * U EA	0	C67531-	Aug-81			
063	8	1A RES 100 OHM 1/4W 5% RCO,F21	RP P 1 P C P EA	0	C67531-	Aug-81			
018	8	1A RES 1K OHM 1/4W 5% P15	RP P 1 P C P EA	0	C67531-	Aug-81			
016	8	1A RES 10K OHM 1/4W 5% 519	RP P 1 P C P EA	0	C67531-	Aug-81			
014	8	1A RES 100 OHM 1/4W 5% 519	RP P 1 P C P EA	0	C67531-	Aug-81			

ITEM LEVEL COMPONENT PART NUMBER

040 8 101-4201

042 8 101-4303

037 8 101-4332

075 8 101-4333

039 8 101-4392

041 8 101-4510

077 8 101-4512

035 8 111-0021

034 8 111-0022

070 8 112-0102

001 8 112-0105

081 8 112-0107

043 8 125-5701

045 8 130-0007

032 8 197-0017

078 8 197-0502

080 8 197-0504

029 8 301-0006

009 8 305-0000

026 8 305-0002

025 8 305-0008

017 8 305-0014

027 8 305-0038

019 8 305-0109

018 8 305-0153

000 8 305-0161

1

FG, PROFILE, \*GENERIC\* DRIVE - USA

UH: EA

ECN: F354

ASSEMBLY QTY: 1

EPC: A SRECT CODE: C TYPE: 1

PLAN CODE: F

DATE: 15-Mar-83

E PART DESCRIPTION

EXTENDED QTY PFF

FOR START DATE

S/R

R9,R10

1A RES 200 OHM 1/4W 5%

R17

1A RES 30R OHM 1/4W 5%

R1,R2,R4,R5

1A RES 3.3K OHM 1/4W 5%

R3,R6,R7,R8,

R11,R12,R13,R18

1A RES 33K OHM 1/4W 5%

R1,R2,R4,R5

1A RES 3.9K OHM 1/4W 5%

R14

1A RES 51 OHM 1/4W 5%

R16

1A RES 5.1K OHM 1/4W 5%

R22

1A RES NETWORK 7 X 2K OHM 5%

RP1

1A RES NETWORK 7 X 10K OHM 5%

RP2

1B RES ARRAY 8 X 47 OHM 10%

1B RES ARRAY 8 X 330 OHM

U1,U2

1B RES ARRAY 8 X 100 OHM

U1,U2

1B CAP ELECT 47 UF -10%+75% 10V

C8,C21,C29,C30

1B CAP CER AXIAL .1 UF +80%-20% 25V

A CRYSTAL, 10MHZ

1A CLOCK OSC,CRYSTAL 10 MHZ (TTL)

1A CLOCK OSCILLATOR,CRYSTAL,10 MHZ

ALT FOR ITEM 78

ALT QTY 1

A IC, 7406

U41

A IC, 74LS00N

U15,U26

A IC, 74LS02N

U31

A IC, 74LS08

U32

A IC, 74LS14

U23

A IC, 74LS38 QUAD 2 INPUT BUFFER

U24

A IC, 74LS109

U37

A IC, 74LS153

U36

A IC, 74LS151

U35

0 C67531-Aug-81

0 C67525-Mar-83

0 C67531-Aug-81

0 C675

0 C67531-Aug-81

0 C67531-Aug-81

0 C67525-Mar-83

0 C67531-Aug-81

0 C67531-Aug-81

0 C67507-Nov-83

0 C77231-Aug-81

0 C93907-Apr-83

0 792 31-Aug-81

0 C57615-Oct-83

0 C58416-Oct-83

0 C06331-Aug-81

0 442 31-Aug-81

0 442 31-Aug-81

0 442 31-Aug-81

0 442 31-Aug-81

0 649 31-Aug-81

0 442 31-Aug-81

0 442 31-Aug-81

0 442 31-Aug-81

0 12-Nov-81

0 06-Nov-83

0 14-Oct-83

INDEPENDIBLE MATERIAL

CUPERTINO OPERATIONS (DIV. 02) RIL VERSION 11-FEB-83 46F 5

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FRST S A P	EXTENDED	ECN	START DATE	CLOSE DATE
020	8 305-0163	A IC, 74LS163	RI P 1 P P P EA	0	442	31-AUG-81	
013	8 305-0174	A IC, 74LS174	RJ P 1 P P P EA	0	442	31-AUG-81	
003	8 305-0240	A IC, 74LS240	RI P 1 B P EA	0	C12731	AUG-81	
002	8 305-0244	A IC, 74LS244	RI P 1 P P P EA	0	442	31-AUG-81	
010	8 305-0257	A IC, 74LS257	RI P 1 P P P EA	0	442	31-AUG-81	
030	8 305-0280	A IC, 74LS280 9-BIT PARITY	RI P 1 P P P EA	0	649	31-AUG-81	
015	8 305-0323	A IC, 74LS323	RI P 1 P P P EA	0	442	31-AUG-81	
047	8 305-0377	A IC, 74LS377	RI P 1 P P P EA	0	442	31-AUG-81	
024	8 307-0074	A IC, 74S74	RI P 1 P P P EA	0	C06331	AUG-81	
011	8 307-0086	A IC, 74S86	RI P 1 P P P EA	0	C06331	AUG-81	
008	8 334-2114	IC IC 1024X4 STATIC RAM 2114 TSTERN	RL P 1 P C P EA	0	C62131	AUG-81	
000	8 062-0083	1B SPEC, 2114 RAM BURN-IN	EX D 7 * U EA	0	C31415	JUL-83	
073	8 335-0004	A FROM, 512 X 8 (UNPROGRAMMED)	RL P 1 P C P EA	0	C43715	JUL-83	
071	8 335-0006	A FROM, MM1 6309-1	RL P 1 P B P EA	0	C02131	AUG-81	12-NOV-81
072	8 335-6309	A FROM, MM1 6309-1	RL P 1 P C P EA	0	642	31-AUG-81	12-NOV-81
012	8 337-8253	MA PROGRAMMABLE INTERVAL TIMER	RL P 1 P A P EA	0	C-6	31-AUG-81	12-NOV-81
004	8 337-8603	B IC SOCKET MICROPRO. W/24P PIGGYBA	RL P 1 * P EA	0	C14831	AUG-81	04-MAY-82
018	8 337-9401	A CRC GENERATOR/CHECKER	RL P 1 P A P EA	0	642	31-AUG-81	
021	8 341-0066	A FROM, U29	RL A 1 * P EA	0	F10513	NOV-81	
022	8 341-0067	A FROM, U37	RL A 1 * P EA	0	F10513	NOV-81	
007	8 341-0068	A RAMPAL	RL P 1 * P EA	0	F10513	NOV-81	
031	8 341-0080	B FROM 2K PROFILE CONTROLLER	RL P 1 * P EA	0	F18413	NOV-81	04-MAY-82
074	8 341-0129	A EFROM-FIRMWARE 3.90 Z8 PROFILE-27	RL A 1 * P EA	0	F11031	AUG-81	12-NOV-81
001	9 335-2716	A EFROM, 2048 X 8 2716	RL P 1 P C P EA	0	642	31-AUG-81	
028	8 351-2074	A QUAD DARLINGTON XSTR ARRAY 2074B	RP P 1 P B P EA	0	642	31-AUG-81	
023	8 359-4024	A VOLTAGE CONTROLLED MULTIVARIABLE	RI P 1 P B P EA	0	642	31-AUG-81	14-OCT-82
043	8 421-4001	1A DIODE RECTIFIER 1N4001 1.00 500	RP P 1 P C P EA	0	C59931	AUG-81	
044	8 421-4120	1A DIODE RECTIFIER 1N4120 1.00 500	RP P 1 P C P EA	0	C59931	AUG-81	



EFFECTIVITY DATE: ALL UNDELIMITED MATERIAL

PARENT PART: 49M0005 1 FG, PROFILE, "GENERIC" DRIVE - USA UM: EA PROD CODE: 0H ABC: \* FLAN CODE: F DATE: 15-Mar-83 ASSEMBLY QTY: 1

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FRST S A P CD C Y P R L U M	EXTENDEH QTY PER	ECH CHR	START DATE	CLOSE DATE
004	7	3A REIDENTIFY SEE 569-0204	RC P 1	0	C523		30-Sep-83
002	6	A CABLE ASSY, #16 AWG GROUND WIRE	P *	0	F18014	Dec-82	
003	7	1B TERMINAL, RING TONGUE #8	P *	0	C34401	Mar-82	
002	7	1A TERMINAL, RECEPT 4.75 X .51 TAB	P *	0	C62801	Mar-82	
001	7	A WIRE, 16 AWG, GRAY, 26/30, 4.80"	X *	0	C05701	Mar-82	
003	6	A ASSY, PCB TSTD, ANALOG	WT A 1	0	F11114	Dec-82	
001	7	1P ASSY, PCB UNTSTD, ANALOG, PROFILE	WU A 1	0	L05031	Aug-81	
000	8	1J SCHEMATIC, ANALOG RFD, PROFILE	D D 7	0	F69701	Mar-82	
050	8	1A RES 1 OHM 1/4W 5% R101	RP P 1 S C P EA	0	C67528	Jul-81	
051	8	1A RES 100 OHM 1/4W 5% R4,67	RP P 1 F C P EA	0	C67528	Jul-81	
053	8	1A RES 1K OHM 1/4W 5% R2-3,R15,R20-21 R38-39,R48,R54,R59 R60-62,R85-88 R106,R108	RP P 1 F C P EA	0	C67528	Jul-81	
068	8	1A RES 10K OHM 1/4W 5% R13,17,42-45,47 R49,70,81,117	RP P 1 F C P EA	0	C67528	Jul-81	
083	8	1A RES 100K OHM 1/4W 5% R115	RP P 1 P C P EA	0	C67528	Jul-81	
080	8	1A RES 110 OHM 1/4W 5% R91,92	RP P 1 C P EA	0	C67528	Jul-81	
077	8	1A RES 120 OHMS 1/4W 5% R25,26	RP P 1 P C P EA	0	C67528	Jul-81	
075	8	1A RES 1.2K OHM 1/4W 5% R107	RP P 1 P C P EA	0	C67528	Jul-81	
072	8	1A RES 12K OHM 1/4W 5% R73	RP P 1 P C P EA	0	C67528	Jul-81	
061	8	1A RES 150 OHM 1/4W 5% R36,68,114	RP P 1 P C P EA	0	C67528	Jul-81	
056	8	1A RES 1.5K OHM 1/4W 5% R7,82,83	RP P 1 P C P EA	0	C67528	Jul-81	
081	8	1A RES 1.8K OHM 1/4W 5% R69	RP P 1 P C P EA	0	C67528	Jul-81	
069	8	1A RES 200 OHM 1/4W 5% R110	RP P 1 P C P EA	0	C67528	Jul-81	
062	8	1A RES 20.0K OHM 1/4W 5% R16,50	RP P 1 P C P EA	0	C76028	Jul-81	
055	8	1A RES 22 OHM 1/4W 5% R23,24,32	RP P 1 P C P EA	0	C67528	Jul-81	
079	8	1A RES 240 OHM 1/4W 5% R18,19	RP P 1 P C P EA	0	C67528	Jul-81	
067	8	1A RES 2.4K OHM 1/4W 5% R80,40,41	RP P 1 P C P EA	0	C67528	Jul-81	
066	8	1A RES 240K OHM 1/4W 5% R39	RP P 1 P C P EA	0	C67528	Jul-81	



EFFECTIVITY DATE: ALL UNIDENTIFIED MATERIAL

PARENT PART: A9M0005 I FG, PROFILE, 'GENERIC' DRIVE USA UM: EA PROD CODE: DH FCN: F354 ASSEMBLY QTY: 1  
ERC: A SECF CODE: G TYPE: J ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	I PART DESCRIPTION	REMARKS	PR ST S A P	EXTENDED QTY PER	CHG	DATE	CHG	DATE	S/N	DATE	S/N
078	8 101-4272	1A RES 2.7K OHM 1/4W 5% R74		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
082	8 101-4301	1A RES 300 OHM 1/4W 5% R111		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
070	8 101-4331	1A RES 330 OHM 1/4W 5% R89,90		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
073	8 101-4332	1A RES 3.3K OHM 1/4W 5% R100,76		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
049	8 101-4390	1A RES 39 OHM 1/4W 5% R78,R112		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
054	8 101-4391	1A RES 390 OHM 1/4W 5% R55		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
060	8 101-4392	1A RES 3.9K OHM 1/4W 5% R9,8,113,1,27 R118,119		RF P 1 P C P EA	0	C67513	Apr-83	C67513	Apr-83			
052	8 101-4471	1A RES 470 OHM 1/4W 5% R37,52-53,77		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
084	8 101-4473	1A RES 47K OHM 1/4W 5% R116,71		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
065	8 101-4511	1A RES 510 OHM 1/4W 5% R63,64,29,30,28		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
071	8 101-4561	1A RES 560 OHM 1/4W 5% R99		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
045	8 101-4681	1A RES 680 OHMS 1/4W 5% R11-12,R22		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
074	8 101-4751	1A RES 750 OHM 1/4W 5% R75,79		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
063	8 101-4752	1A RES 7.5K OHM 1/4W 5% R5,6,33,34		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
076	8 101-4822	1A RES 8.2K OHM 1/4W 5% R72		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
057	8 101-4823	1A RES 82K OHM 1/4W 5% R46		RF P 1 P C P EA	0	C67528	Jul-81	C67528	Jul-81			
048	8 108-1543	1A RES 1.54K OHM 1/4W 1% R84		RF P 1 P C P EA	0	C75828	Jul-81	C75828	Jul-81			
042	8 108-1783	1A RES 1.78K OHM 1/4W 1% R10		RF P 1 P C P EA	0	C75828	Jul-81	C75828	Jul-81			
041	8 108-1963	1A RES 1.96K OHM 1/4W 1% R105,104		RF P 1 P C P EA	0	C75801	Mar-82	C75801	Mar-82			
047	8 108-3833	1A RES 3.83K OHM 1/4W 1% R93,R95-96,R97		RF P 1 P C P EA	0	C75831	Jul-81	C75831	Jul-81			
039	8 108-3923	1A RES 3.92K OHM 1/4W 1% R65,66		RF P 1 P C P EA	0	C75828	Jul-81	C75828	Jul-81			
046	8 108-4531	1A RES 45.3 OHM 1/4W 1% R14		RF P 1 P C P EA	0	C75828	Jul-81	C75828	Jul-81			
043	8 108-5423	1A RES 5.42K OHM 1/4W 1% R94,R93		RF P 1 P C P EA	0	C75828	Jul-81	C75828	Jul-81			
106	8 109-0063	W POT. 10M 1% OHM 202		RF P 1 P C P EA	0	442	10-Oct-84	442	10-Oct-84			
040	8 109-0060	W POT. 10M 50% OHM 202		RF P 1 P C P EA	0	C04513	May-82	C04513	May-82			

EFFECTIVITY DATE: null  
 PARENT PART: ASM0005  
 1 FG, PROFILE, "GENERIC" DRIVE - USA UM: EA PRD CODE: DH ECR: F354 ASSEMBLY QTY: 1  
 ERC: A SRCE CODE: G TYPE: 1 ARC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	REMARKS	FR S T S A P	CH C Y P R L U M	EXTENDED QTY PER	ECN	START DATE	CLOSE DATE	S/N
098	8 109-0410	1A POT, 500 OHM 18 - 25 TURNS		RF P 1	C P EA	0	C50428	Jul-81	02-Mar-82	
099	8 109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS		RF P 1	C P EA	0	F10513	May-82	09-Oct-83	
038	8 111-0023	1A RFS NETWORK 7 X 560 OHM 5% ALTN P/N FOR ITEM 40		RF P 1	C P EA	0	C67528	Jul-81		
094	8 111-0024	1A RES NETWORK 7 X 4.7K OHM 5% RF-1		RF P 1	C P EA	0	C67528	Jul-81		
059	8 127-0100	1B CAP TANT 4.7 uF 20% 10V C59		RF P 1	* P EA	0	C59928	Jul-81		
037	8 127-0101	1B CAP TANT 10 uF 20% 15/16V C38-C40		RF P 1	* P EA	0	C59928	Jul-81		
029	8 130-0002	1B CAP CER AXIAL .01 uF +80%-20% 25V C12,6,7		RF P 1	F C P EA	0	C93928	Jul-81		
097	8 130-0003	1B CAP CER AXIAL .1 uF +80%-20% 25V C13,C14		RF P 1	F C P EA	0	C939		14-Apr-83	
028	8 130-0007	1B CAP CER AXIAL .1 uF +80%-20% 25V C3-5,10-16,21,22,25, C27,35-37,42-45,47		RF P 1	C P EA	0	C93901	Mar-82		
031	8 130-0200	1A CAP CER .001 uF 10% 25V C24, C32		RF P 1	C P EA	0	C59928	Jul-81		
030	8 130-0201	1A CAP CER .0022 uF 10% 25V C19,23,28-31,26,62		RF P 1	C P EA	0	C59928	Jul-81		
036	8 137-5401	1A CAP DIP MICA 20 pF 5% 500V C61		RF P 1	C P EA	0	C54128	Jul-81		
035	8 137-5701	1A CAP DIP MICA 47 pF 5% 500V C34		RF P 1	C P EA	0	C54128	Jul-81		
034	8 137-5801	1A CAP DIP MICA 75 pF 5% 500V C8		RF P 1	C P EA	0	C54128	Jul-81		
032	8 137-6101	1A CAP DIP MICA 100 pF 5% 500V C33		RF P 1	C P EA	0	C54128	Jul-81		
033	8 137-6301	1A CAP DIP MICA 150 pF 5% 500V C9, C18, C17, C20		RF P 1	C P EA	0	C54128	Jul-81		
027	8 151-4701	1C INDUCTOR, 5.6 uH 10% L1, L2		RF P 1	* P EA	0	C39528	Jul-81		
021	8 156-0100	A DELAY LINE 14 PIN DIP 100 OHM, 50 DLY 2		RF P 1	* P EA	0	792 28	Jul-81		
022	8 156-0110	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1		RF P 1	* P EA	0	792 28	Jul-81		
007	8 301-0045	A IC, 7445 U4		RF P 1	C P EA	0	C06328	Jul-81		
001	8 301-0074	A IC, 7474 U2		RF P 1	F C P EA	0	C06328	Jul-81		
005	8 305-0014	A IC, 74LS14 U30		RF P 1	F B P EA	0	442 28	Jul-81		
002	8 305-0174	A IC, 74LS174 U29		RF P 1	F B P EA	0	442 28	Jul-81		
004	8 307-0064	A IC, 74S64 U27		RF P 1	B P EA	0	C06328	Jul-81		
017	8 309-0102	A MUX 8 THRU 00P DATA		RF P 1	C P EA	0	741 28	Jul-81		

INVENTORY OF MATERIAL

PARENT PART: A9M0005 1 FG, PROFILE, \*GENFRIC\* DRIVE - USA UM: EA PROD CODE: DH ECN: P354 ASSEMBLY QTY: 1  
ERC: A SRCE CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FF	ST	SA	AP	EXTENDED	ECN	START	CLOSE
		REMARKS	CP	Y	P	R	UM	CHG	DATE	DATE
			QTY	PER	UM	QTY	PPR		S/N	S/N
010	8 325-0107	A TRIPLE 2-INFT EXCL OR/EXCL NOR GA RI P 1 C P EA U18 U10, U15					0	741	28-Jul-81	
008	8 325-0114	A TRIPLE LINE RECEIVER U5, U14	RI	P	1	C	P	EA	741	28-Jul-81
009	8 325-0116	A TRIPLE LINE RECEIVER U26, U9	RI	P	1	C	P	EA	741	28-Jul-81
012	8 325-0117	A DL 2-WID 2-3-INFT OR-AND/OR-AND-I RI P 1 C P EA U16	RI	P	1	C	P	EA	741	28-Jul-81
011	8 325-0131	R IC ECL HIGH SPEED DUAL D FIIP-FLO RI P 1 C P EA U11,17,19,20,21,22	RI	P	1	C	P	EA	C25528	Jul-81
006	8 327-0453	A IC, DUAL PERIPHERAL DRIVES U3	RI	P	1	* P	EA	0	757	28-Jul-81
096	8 335-0007	A PROG HEX 16 INPT REG AND-OR GT AR RL P 1 P B P EA	RL	A	1	* P	EA	0	642	28-Jul-81
003	8 341-0069	A MFMAL PROG HEX 16 INPT REG AND-OR GT ARY U28	RL	A	1	* P	EA	0	P10501	Mar-82
014	8 351-2907	A IC TRANS ARRAY QUAD FNF GEN PURPO RP P 1 C P EA U31, U23, U12	RP	P	1	C	P	EA	750	28-Jul-81
016	8 351-3127	A TRANSISTOR,ARRAY NFN HIGH FREQ. U7	RP	P	1	C	P	EA	750	28-Jul-81
023	8 351-6700	A IC, TRANS. ARRAY QUAD COMP. PAIRS RI P 1 C P EA U1, U24	RI	P	1	C	P	EA	750	28-Jul-81
058	8 353-0005	A IC REG. +5V 100MA TO 92, 3 TERMNL RI P 1 C P EA RG1	RI	P	1	C	P	EA	792	28-Jul-81
018	8 353-0319	A IC, HIGH SPEED DUAL COMPARATOR U13	RI	P	1	C	P	EA	750	28-Jul-81
017	8 353-0353	A DUAL FET OP AMP/BUFFER U25,U8	RP	P	1	C	P	EA	750	28-Jul-81
015	8 353-0592	A IC, VIDEO AMPLIFIER U6	RI	P	1	C	P	EA	750	28-Jul-81
024	8 371-4152	1A DIODE FAST SWITCH 1N4152 500mW 30 RP P 1 C P EA CR1-14, CR16-21, CR23-24, CR26	RP	P	1	C	P	EA	C53828	Jul-81
100	8 372-2222	1A TRANS,NFN,SWITCHING AND AMP 2N222 ALT P/N FOR ITEM 23 U1-QTY 2	* *	* *	* *	* *	EA	0	C40308	Jul-83
101	8 372-2907	A XSTR,2N2907, FNF SWITCH & AMPLIFI ALT P/N FOR ITEM 23 U1-QTY 2	* *	* *	* *	* *	EA	0	C25908	Jul-83
102	8 372-3904	A TRANSISTOR,NFN SW.&AMP. 2N3904 ALT P/N FOR ITEM 23 U24-QTY 2	RP	P	1	P	C	P	EA	0
103	8 372-3504	1F TRANSISTOR,NFN SW.&AMP. 2N3904 ALT P/N FOR ITEM 23 U24-QTY 2	RP	P	1	P	C	P	EA	0
026	8 375-0019	1A DIODE REFERENCE 10mA 1.5V CR1	RP	P	1	C	P	EA	0	0

EFFECTIVITY DATE: ALL INDEPENDENT MATERIAL

PARENT PART: APM0005 1 FG, PROFILE, "GENERIC" DRIVE - USA UM: EA PROD CONF: DH ECH: F354 ASSEMBLY QTY: 1, SRC CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FR ST I S A P CD C Y P B L UM	EXTENDED QTY PER	ECH CHG	START DATE	CLOS DATE	S/N
019	8	375-0012	1A DIODE DUAL VOLT VAR CAP 200mA 32V	RP P 1 * P EA	0	C53828	Jul-81		
020	8	376-0016	A FET, N-CHANNEL VOLT CONTRL FETIS, Q2	RP P 1 * P EA	0	C30328	Jul-81		
090	8	511-0801	C SOCKET, IC 8 PIN	RP P 1 P C P EA	0	799	28-Jul-81	14-Apr-83	
091	8	511-1401	C SOCKET, IC 14 PIN	RP P 1 P C P EA	0	799	28-Jul-81	14-Apr-83	
092	8	511-1601	C SOCKET, IC 16 PIN	RP P 1 P C P EA	0	799	28-Jul-81	14-Apr-83	
093	8	511-2001	C SOCKET, IC 20 PIN	RP P 1 P C P EA	0	799	28-Jul-81	14-Apr-83	
089	8	515-0005	1B CONN, PIN, SINGLE	RP P 1 P C P EA	0	C78128	Jul-81		
087	8	515-0120	1A CONN, HDR, SGL ROW, 4P	RP P 1 * P EA	0	C78128	Jul-81	02-Mar-82	
085	8	515-0130	1B CONN, HDR, RT ANG, DBL ROW, 8/16P	RP P 1 * P EA	0	C78128	Jul-81		
088	8	515-0131	1B CONN, HDR, RT ANG, DBL ROW, 17/34P	RP P 1 C P EA	0	C78101	Mar-82	28-Aug-83	
086	8	515-0140	1A CONN, HDR, RT ANG, 5P, W/LKG RAMP	RP P 1 * P EA	0	C78128	Jul-81		
105	8	515-0380	1A CONN, HDR, RT ANG, DBL ROW, 17/34P	* * * * EA	0	C78129	Aug-83		
104	8	550-0101	1C TUBING, HEAT SHRINK 1/4 ID BLACK USE W/ALT P/N	EX X 7 P C P FT	0	C50308	Jul-83		
095	8	820-0054	AE PCB, ANALOG PROFILE	RP P 1 * P EA	0	P21401	Mar-82		
001	6	699-0054	A ASSY, O.E.M. HEAD DISC (H.D.A.)	VX A 1 P A P EA	0	600	14-Dec-82		
006	4	810-0090	1A DRESS PANEL, DRIVE, PROFILE	RM P 1 * P EA	0	P56714	Dec-82		
007	4	810-0091	1B DRESS PANEL, PWR SPLY PROFILE	RM P 1 * P EA	0	P64414	Dec-82		
012	4	825-0207	B LABEL, FCC NON COMPLIANCE APPL 3	EX X 7 P C P EA	0	P59321	Mar-83		
004	3	656-6121	3R INACT. ASSY, CHASSIS, PROFILE-CLASS	* * * * EA	1	L30512	Dec-83		
003	4	400-1606	1C SCR 6-32X3/8 PN HD CRS REC STL ZN	EX X 1 P C P EA	1	C54012	Dec-83		
013	4	403-1606	1C SCR 6-32X3/8 PN CRS REC STL BL ZI	EX X 7 S C P EA	16	C54012	Dec-83		
009	4	430-1001	1C SCR TAP 8-18X.437 PN CRS STL ZN	EX X 7 P C P EA	3	C54012	Dec-83		
002	4	656-5121	3A INACT. SUBASSY, BASE, PROFILE-CLASS	* * * * EA	1	L30512	Dec-83		
005	5	400-1604	1C SCR 6-32X1/4 PN HD CRS REC STL ZN	EX X 7 C P EA	2	C54012	Dec-83		
011	5	400-1608	1C SCR 6-32X1/2 PN HD CRS REC STL 7N	EX X 7 C P EA	1	C54012	Dec-83		
012	5	436-1006	1C SCR TAP 4-24X.250 PN CRS REC STL	* * * * EA	1	C54012	Dec-83		
001	5	699-5010	1A PURCH ASSY, COATD BTM CVR, PRFLE-B	* * * * EA	1	F67612	Dec-83		
001	6	656-5021	6A SUBASSY COVER, BOTTOM, PROFILE	* * * * EA	1	F40812	Dec-83		
002	7	805-0086	1A SHIELD, CSA PROFILE	* * * * EA	1	F40801	Apr-83		
001	7	815-5008	1C COVER, BOTTOM, PROFILE	RM P 1 * P EA	1	F40801	Apr-83		
008	5	805-0104	A SUPPORT, PROFILE	RP P 1 * P EA	1	F16812	Dec-83		
002	5	805-5022	1A SURFANEL, REAR, PROFILE	* * * * EA	1	F64412	Dec-83		
003	5	810-0095	1A COVER DRIVE, BOTTOM, PROFILE	* * * * EA	1	F40812	Dec-83		
004	5	865-0005	MA FOOT, .52HT, SQ	* * * * EA	6	545	12-Dec-83		
015	4	656-5130	3D INACT. MFG SUBASSY, COVER, PROFILE	EX X 7 P C P EA	1	L30506	Jan-84		
004	5	590-0047	1B CARLE, ASSY, LED, PROFILE	RC P 1 * P EA	1	F46414	Dec-82		
008	6	517-0001	1A CONN, RCPT, INSUL, DJSPL, 7P	EX X 7 * U IN	24,5000	F10931	Aug-81		
003	6	550-0010	A TUBING, BRAINED, 1/8 DIA.	EX X 7 * P C P FT	25	C50331	Aug-81		
007	6	550-0101	1C TUBING, HEAT SHRINK 1/4 ID BLACK	EX X 7 P C P FT	25	C50331	Aug-81		
006	6	550-0103	1C TUBING, HEAT SHRINK 1/16 ID BLACK	EX X 7 P C P FT	25	C50331	Aug-81		
004	6	561-2600	R WIRE, BLACK 26 AWG, 7 X 34	EX X 7 P * P FT	25	764	31-Aug-81		
005	6	561-2622	P WIRE, 26 AWG STEEL, 2P	EX X 7 * U FT	25	C01331	Aug-81		

EFFECTIVITY DATE: ALL J O D E N T E D B I L L S O F M A T E R I A L

PARENT PART: A9R0005

1 FG, PROFILE, 'GENERIC' DRIVE - USA UM: EA  
ERC: A SRCL CODE: G TYPE: 1 ARC: \*

ECN: P354 ASSEMBLY QTY: 1  
DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	F PART DESCRIPTION REMARKS	QTY	U	M	EXTENDED QTY	FF	ECN CHG	DATE	START DATE	S/N	CLOSE DATE	S/N
001	6	710-0004	MA LED, RED APPLE III DISKABLE	RF	X	1	P	C	P	EA	1	552	31-Aug-81
002	6	815-0190	0 GROMET, PANEL MTG. FOR RECT. LAMP	RM	X	1	P	C	P	EA	0	442	31-Aug-81
001	5	699-5011	1R FURCH ASSY. COATD TOP CVR, PKFLE-B	RM	*	*	*	*	*	EA	1	L05112	Dec-83
001	6	815-5007	1C COVER, TOP, PROFILE	RM	P	1	*	*	*	EA	1	F40812	Dec-83
008	5	815-0190	0 GROMET, PANEL MTG. FOR RECT. LAMP	RM	X	1	P	C	P	EA	1	442	27-Apr-83
009	5	815-5007	1C COVER, TOP, PROFILE	RM	P	1	*	*	*	EA	0	P408	
005	5	825-0311	1B LABEL, LOGO 16MM BY 16MM	EX	X	7	P	C	P	EA	1	P51414	Dec-82
006	5	825-0313	1B LABEL, NAMEPLATE, PROFILE	EX	X	7	P	C	P	EA	1	P51414	Dec-82
007	5	825-0315	1C LABEL, LFD PROFILE	EX	P	7	*	*	*	EA	1	P51414	Dec-82
003	5	830-0025	3A INACTIVE, REIDENTIFIED SEE 830-002	X	X	*	*	*	*	EA	2	C61114	Dec-82
002	5	835-0005	1R NUT, SPEED 'J' TYPE SIZE 8	EX	X	7	P	C	P	EA	3	C74414	Dec-82
001	4	656-5151	3A INACT. SUBASY, HDA/PWR SUP, PREL-CLS	X	X	*	*	*	*	EA	1	L30512	Dec-83
004	5	159-0001	B TOROID, FERRITE	EX	P	1	P	C	P	EA	2	C-4	12-Dec-83
003	5	341-0171	A MICROPKCSR-2K PROG ROM FORR PROFIL	X	X	*	*	*	*	EA	1	P26612	Dec-83
001	5	656-5111	3B INACT. SUBASY, PWR SPLY, PROFLE-CLS	X	X	*	*	*	*	EA	1	L30512	Dec-83
007	6	400-1603	1C SCR 6-32X3/16 FN HD CRS REC STL Z	EX	P	7	*	*	*	EA	1	C54012	Dec-83
008	6	400-1606	1C SCR 6-32X3/8 FN HD CRS REC STL Z	EX	X	1	P	C	P	EA	1	C54012	Dec-83
009	6	564-0010	1A STRAP, GROUND, BRAIDED, 2.75" LON	X	X	*	*	*	*	EA	1	C70712	Dec-83
006	6	656-4102	MC ASSY, PCB TSTD, CONTROLLER	WT	A	1	*	*	*	EA	1	P26612	Dec-83
002	7	337-8603	B IC SOCKET MICROPRO. W/24P PIGGYBA	RL	P	1	*	*	*	EA	1	C14805	May-82
U25													
001	7	656-0102	1M ASSY, PCB, UNTSTD, CONTROLLER, PROFIL	WU	A	1	*	*	*	EA	1	P65131	Aug-81
000	8	050-5006	1E SCHEMATIC, CONTROLLER R0, PROFILE	D	7	*	U	EA	0			P65104	Jan-82
063	8	101-4101	1A RES 100 OHM 1/4W 5%	RP	P	1	P	C	P	EA	2	C67531	Aug-81
R20, R21													
038	8	101-4102	1A RES 1K OHM 1/4W 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
R15													
016	8	101-4103	1A RES 10K OHM 1/4W 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
R19													
036	8	101-4152	1A RES 1.5K OHM 1/4W 5%	RP	P	1	P	C	P	EA	2	C67531	Aug-81
R9, R10													
040	8	101-4201	1A RES 200 OHM 1/4W 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
R17													
042	8	101-4303	1A RES 30K OHM 1/4W 5%	RP	P	1	P	C	P	EA	4	C67525	Mar-83
R1, R2, R4, R5													
037	8	101-4332	1A RES 3.3K OHM 1/4W 5%	RP	P	1	P	C	P	EA	8	C67531	Aug-81
R3, R6, R7, R8,													
R11, R12, R13, R18													
075	8	101-4333	1A RES 33K OHM 1/4W 5%	RP	P	5	P	C	P	EA	4	C675	
R1, R2, R4, R5													
039	8	101-4392	1A RES 3.9K OHM 1/4W 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
R14													
041	8	101-4510	1A RES 51 OHM 1/4W 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
R16													
077	8	101-4512	1A RES 5.1K OHM 1/4W 5%	RP	P	1	P	C	P	EA	1	C67525	Mar-83
R22													
045	8	111-0021	1A RES NETWORK 7 x 2K OHM 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
RPI													
044	8	111-0022	1A RES NETWORK 7 x 10K OHM 5%	RP	P	1	P	C	P	EA	1	C67531	Aug-81
RPI													

EFFECTIVITY DATE: ALL J N D F M T E D B I L L S O F M A T E R I A L

PARENT PART: A9H0005 1 FG, PROFILE, 'GENERIC' DRIVE - USA UM: EA PROD CODE: DH ECH: F354 ASSEMBLY QTY: 1  
ERC: A SRCO CODE: G TYPE: 1 ARC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR S T S A P	EXTENDED QTY PER	FCN CHG	START DATE	CLOSE DATE	S/N
070	8 112-0102	1B RES ARRAY 8 X 47 OHM 10% REMARKS: U1,U2	RF P 1 P C P EA	2	C67531	AUG-81	12-NOV-81	
001	8 112-0105	1B RES ARRAY 8 X 330 OHM REMARKS: U1,U2	RF P 1 * P EA	2	C67513	NOV-81	06-NOV-83	
081	8 112-0107	1B RES ARRAY 8 X 100 OHM REMARKS: U1,U2	* * * * EA	2	C67507	NOV-83		
043	8 125-5701	1B CAP ELECT 47 UF -10%+75% 10V REMARKS: C8,C21,C29,C30	RF P 1 C P EA	4	C77231	AUG-81		
045	8 130-0007	1B CAP CER AXIAL .1 UF +80%-20% 25V REMARKS: A CRYSTAL, 10MHZ	RF P 1 C P EA	31	C93907	APR-83		
032	8 197-0017	1A CLOCK OSC,CRYSTAL 10 MHZ (TTL) REMARKS: U15,U26	EX P 7 * P EA	1	792 31	AUG-81		
078	8 197-0502	1A CLOCK OSCILLATOR,CRYSTAL,10 MHZ REMARKS: U31	* * * * EA	1	C57615	OCT-83		
080	8 197-0504	1A CLOCK OSCILLATOR,CRYSTAL,10 MHZ REMARKS: ALT FOR ITEM 78	* * * * EA	0	C58416	OCT-83		
029	8 301-0006	A IC, 7406 REMARKS: U41	EX P 7 * P EA	1	C06331	AUG-81		
009	8 305-0000	A IC, 74LS00N REMARKS: U15,U26	RI P 1 P B P EA	2	442 31	AUG-81		
026	8 305-0002	A IC, 74LS02N REMARKS: U31	RI P 1 P B P EA	1	442 31	AUG-81		
025	8 305-0008	A IC, 74LS08 REMARKS: U32	RI P 1 P B P EA	1	442 31	AUG-81		
017	8 305-0014	A IC, 74LS14 REMARKS: U23	RI P 1 P B P EA	1	442 31	AUG-81		
027	8 305-0038	A IC, 74LS39 QUAD 2 INPUT BUFFER REMARKS: U24	RI P 1 P B P EA	1	649 31	AUG-81		
019	8 305-0109	A IC, 74LS109 REMARKS: U36	RI P 1 P B P EA	1	442 31	AUG-81		
014	8 305-0153	A IC, 74LS153 REMARKS: U6	RI P 1 P B P EA	1	442 31	AUG-81		
006	8 305-0161	A IC, 74LS161 REMARKS: U10,U16,U17	RI P 1 P B P EA	3	442 31	AUG-81		
020	8 305-0163	A IC, 74LS163 REMARKS: U22	RI P 1 P B P EA	1	442 31	AUG-81		
013	8 305-0174	A IC, 74LS174 REMARKS: U30,U34,U38	RI P 1 P B P EA	3	442 31	AUG-81		
003	8 305-0240	A IC, 74LS240 REMARKS: U9	RI P 1 B P EA	1	C12731	AUG-81		
002	8 305-0244	A IC, 74LS244 REMARKS: U4,U5	RI P 1 P B P EA	2	442 31	AUG-81		
010	8 305-0257	A IC, 74LS257 REMARKS: U13,U20	RI P 1 P B P EA	2	442 31	AUG-81		
030	8 305-0280	A IC, 74LS280 9-BIT PARITY REMARKS: U3	RI P 1 P B P EA	1	649 31	AUG-81		
015	8 305-0323	A IC, 74LS323 REMARKS: U14	RI P 1 P B P EA	1	442 31	AUG-81		
047	8 305-0377	A IC, 74LS377 REMARKS: U21	RI P 1 P B P EA	1	442 31	AUG-81		
024	8 307-0074	A IC, 74LS74 REMARKS: U19	RI P 1 P B P EA	1	C06331	AUG-81		
011	8 307-0086	A IC, 74LS86 REMARKS: U19	RI P 1 P B P EA	1	C06331	AUG-81		

EFFECTIVITY DATE: ALL IDENTIFIED MATERIAL

PARENT PART: A9M0005 1 FG, PROFILE, \*GENERIC\* DRIVE - USA UM: EA PROD CODE: DH ECN: P354 ASSEMBLY QTY: 1  
ERC: A SRCE CODE: G TYPE: 1 ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	REMARKS	FR ST S A P	UM	EXTENDED	ECN	START	CLOSE
				U D L Y P R L U M		QTY PER	CHG	DATE	S/N
008	8 334-2114	1C IC 1024x4 STATIC RAM 2114 TST&ERN RI P 1 P C P EA	U28 U11,U18			2	C62131	AUG-81	
000	9 062-0083	1B SPEC, 2114 RAM BURN-IN		EX D 7 * U E A		0	C31415	JUL-83	
001	9 333-2114	1B IC 1024 X 4 STATIC RAM 2114		RL P 1 C P EA		0	C43715	JUL-83	
073	8 335-0004	A PROM, 512 X 8 (UNPROGRAMMED)		RL P 1 P C P EA		1	C02131	AUG-81	12-Nov-81
071	8 335-0006	A PROG OCT 16 INPT AND-OR-INVT GT A		RL P 1 P B P EA		1	642 31	AUG-81	12-Nov-81
072	8 335-6309	A PROM, MMI 6309-1		RL P 1 P C P EA		1	C-6 31	AUG-81	12-Nov-81
012	8 337-8253	MA PROGRAMMABLE INTERVAL TIMER		RL P 1 P A P EA		1	642 31	AUG-81	
004	8 337-8603	B IC SOCKET MICROPRO, W/24P PIGGYBA RI P 1 * P EA	U33			1	C14831	AUG-81	04-May-82
018	8 337-9401	A CRC GENERATOR/CHECKER	U25	RL P 1 P A P EA		1	642 31	AUG-81	
021	8 341-0066	A PROM, U29	U35	RL A 1 * P EA		1	P10513	NOV-81	
022	8 341-0067	A PROM, U37	(MMI 6309-1)	RL A 1 * P EA		1	F10513	NOV-81	
007	8 341-0068	A RAMPAL		RL P 1 * P EA		1	P10513	NOV-81	
031	8 341-0080	B PROG PROM 2K PROFILE CONTROLLER	U27 (OCT 16 INPT AND-OR-INVT GT ARY)	RL P 1 * P EA		1	F18413	NOV-81	04-May-82
074	8 341-0129	A EPROM-FIRMWARE 3.90 Z8 PROFILE-27		RL A 1 * P EA		1	P11031	AUG-81	12-Nov-81
001	9 335-2716	A EPROM, 2048 X 8 2716		RL P 1 P C P EA		1	642 31	AUG-81	
028	8 351-2074	A QUAD DARLINGTON XSTR ARRAY 2074B		RP P 1 P B P EA		2	642 31	AUG-81	
023	8 359-4024	A VOLTAGE CONTROLLED MULTIVIBRATOR	U7,U8	RI P 1 P B P EA		1	642 31	AUG-81	14-Oct-83
033	8 371-4001	1A DIODE RECTIFIER IN4001 1.0A 50V	U40	RP P 1 P C P EA		8	C59331	AUG-81	
076	8 371-4128	1A DIODE ZENER IN4128 250mW 60V	CR1-CR8	RP P 1 * P EA		4	C53831	AUG-81	12-Nov-81
064	8 371-4148	A DIODE FAST SWITCH IN4148 200mA 75		RP P 1 P C P EA		4	C53813	NOV-81	
062	8 400-1406	1C SCR 4-40X3/8 FN HD CRS REC STI ZN	CR9-CR12	EX X 7 P C P EA		2	C54031	AUG-81	
055	8 511-1401	C SOCKET, IC 14 PIN		RP P 1 P C P EA		3	799 07	APR-83	
056	8 511-1601	C SOCKET, IC 16 PIN		RP P 1 P C P EA		11	799 31	AUG-81	
057	8 511-1801	C SOCKET, IC 18 PIN		RP P 1 P C P EA		2	799 31	AUG-81	
058	8 511-2001	C SOCKET, IC 20 PIN		RP P 1 P C P EA		7	799 31	AUG-81	
059	8 511-2401	C SOCKET, IC 24 PIN		RP P 1 P C P EA		1	799 31	AUG-81	
060	8 511-4001	C SOCKET, IC 40 PIN		RP P 1 P C P EA		1	799 31	AUG-81	
061	8 515-0005	1R CONN,PIN,SINGLE		RP P 1 P C P EA		9	C78131	AUG-81	
054	8 515-0053	1C CONN,HDR,STR,2P		RP P 1 P C P EA		1	C78131	AUG-81	
053	8 515-0082	1A HEADER, 10 PIN RT ANGLE W/O EARS	F7	RP P 1 C P EA		1	C48031	AUG-81	16-Nov-82
066	8 515-0150	1A CONN,HDR,RT ANG,5P,156 STR,W/LOC	F5	RP P 1 * P EA		1	C78113	NOV-81	
067	8 515-0160	1A CONN,HDR,RT ANG,5P,W/LOC RAMP	F3	RP P 1 * P EA		1	C78113	NOV-81	
065	8 519-0160	1B CONN,FC TAIL,90 DEG,NET,LNC FTREI	F4	RP P 1 * P EA		1	C78113	NOV-81	





EFFECTIVITY DATE: ALL INVENTED RILLS OF MATERIAL

PARENT PART: A9M0005 1 FG, PROFILE, 'GENERIC' DRIVE USA UM: EA PROD CODE: DH FCN: F354 ASSEMBLY QTY: 1  
ERC: A SRCE CONF: G TYPE: 1 ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR S T S A F C P C Y P B L U M	EXTENDED QTY PER	ECN CHG	START DATE	CLOSE DATE	S/N
056	8 101-4182	1A RES 1.8K OHM 1/4W 5Z R69	RP P 1 P C P EA	1	C67528	Jul-81		
081	8 101-4201	1A RES 200 OHM 1/4W 5Z R110	RP P 1 P C P EA	1	C67528	Jul-81		
069	8 101-4203	1A RES 20.0K OHM 1/4W 5Z R16,50	RP P 1 P C P EA	2	C76028	Jul-81		
062	8 101-4220	1A RES 22 OHM 1/4W 5Z R23,24,32	RP P 1 P C P EA	3	C67528	Jul-81		
055	8 101-4241	1A RES 240 OHM 1/4W 5Z R18,19	RP P 1 P C P EA	2	C67528	Jul-81		
079	8 101-4242	1A RES 2.4K OHM 1/4W 5Z R80,40,41	RP P 1 P C P EA	3	C67528	Jul-81		
067	8 101-4243	1A RES 24K OHM 1/4W 5Z R35	RP P 1 P C P EA	1	C67528	Jul-81		
066	8 101-4244	1A RES 240K OHM 1/4W 5Z R31	RP P 1 P C P EA	1	C67528	Jul-81		
078	8 101-4272	1A RES 2.7K OHM 1/4W 5Z R74	RP P 1 P C P EA	1	C67528	Jul-81		
082	8 101-4301	1A RES 300 OHM 1/4W 5Z R111	RP P 1 P C P EA	1	C67528	Jul-81		
070	8 101-4331	1A RES 330 OHM 1/4W 5Z R89,90	RP P 1 P C P EA	2	C67528	Jul-81		
073	8 101-4332	1A RES 3.3K OHM 1/4W 5Z R100,76	RP P 1 P C P EA	2	C67528	Jul-81		
049	8 101-4390	1A RES 39 OHM 1/4W 5Z R78,R112	RP P 1 P C P EA	2	C67528	Jul-81		
054	8 101-4391	1A RES 390 OHM 1/4W 5Z R55	RP P 1 P C P EA	1	C67528	Jul-81		
060	8 101-4392	1A RES 3.9K OHM 1/4W 5Z R98,113,1,27 R118,119	RP P 1 P C P EA	7	C67513	Apr-83		
052	8 101-4471	1A RES 470 OHM 1/4W 5Z R37,52-53,77	RP P 1 P C P EA	4	C67528	Jul-81		
084	8 101-4473	1A RES 47K OHM 1/4W 5Z R116,71	RP P 1 P C P EA	2	C67528	Jul-81		
065	8 101-4511	1A RES 510 OHM 1/4W 5Z R63,64,29,30,28	RP P 1 P C P EA	5	C67528	Jul-81		
071	8 101-4561	1A RES 560 OHM 1/4W 5Z R99	RP P 1 P C P EA	1	C67528	Jul-81		
045	8 101-4681	1A RES 680 OHMS 1/4W 5Z R11-12,R22	RP P 1 P C P EA	3	C67528	Jul-81		
074	8 101-4751	1A RES 750 OHM 1/4W 5Z R75,79	RP P 1 C P EA	2	C67528	Jul-81		
063	8 101-4752	1A RES 7.5K OHM 1/4W 5Z R5,6,33,34	RP P 1 P C P EA	4	C67528	Jul-81		
074	8 101-4820	1A RES 8.2K OHM 1/4W 5Z R72	RP P 1 P C P EA	1	C67528	Jul-81		
057	8 101-4823	1A RES 82K OHM 1/4W 5Z R46	RP P 1 C P EA	1	C67528	Jul-81		
048	8 101-4844	1A RES 1.54K OHM 1/4W 1Z	RP P 1 C P EA	1	C67528	Jul-81		

EFFECTIVITY DATE: ALL

PARENT PART: 09M0005

1 FG, PROFILE, 'GENERIC' DRIVE - USA  
ERC: A SRC CODE: G TYPE: 1

UH: FA PROD CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ABC: \* PLAN CODE: F DATE: 15-Mar-83

INVENTORY BILL OF MATERIAL

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	REMARKS	FF ST S A F	EXTENDED QTY PER	ECN CHG	START DATE	CLOSE DATE
042	8 108-1783	1A RES 1.78K OHM 1/4W 1% R84		RP P 1 C P EA	1	C75828	Jul-81	
041	8 108-1963	1A RES 1.96K OHM 1/4W 1% R10		RP P 1 * P EA	2	C75801	Mar-82	
047	8 108-3833	1A RES 3.83K OHM 1/4W 1% R105,104		RP P 1 * P EA	4	C75831	Jul-81	
039	8 108-3923	1A RES 3.92K OHM 1/4W 1% R93,R95-96,R97		RP P 1 P C P EA	2	C75828	Jul-81	
046	8 108-4531	1A RES 45.3 OHM 1/4W 1% R65,66		RP P 1 C P EA	1	C75828	Jul-81	
043	8 108-5623	1A RES 5.62K OHM 1/4W 1% R14		RP P 1 C P EA	2	C75828	Jul-81	
106	8 109-0002	0 POT, TRIM 1K OHM 20% R94,R98		RP P 1 P C P EA	1	442	10-Oct-83	09-Oct-83
040	8 109-0005	A POT, TRIM 500 OHM, 20% ALTN P/N 109-0420		RP P 1 * P EA	1	C04518	May-82	
098	8 109-0410	1A POT, 500 OHM 18 - 25 TURNS		RP P 1 C P EA	1	C50428	Jul-81	02-Mar-82
099	8 109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS ALTN P/N FOR ITEM 40		RP P 1 C P EA	0	F10518	May-82	09-Oct-83
038	8 111-0023	1A RES NETWORK 7 X 560 OHM 5% RP2-B		RP P 1 C P EA	7	C67528	Jul-81	
094	8 111-0024	1A RES NETWORK 7 X 4.7K OHM 5% RP-1		RP P 1 C P EA	1	C67528	Jul-81	
059	8 127-0100	1B CAP TANT 4.7 uF 20% 10V C59		RP P 1 * P EA	1	C59928	Jul-81	
037	8 127-0101	1B CAP TANT 10 uF 20% 15/16V C38-C40		RP P 1 * P EA	3	C59928	Jul-81	
029	8 130-0002	1B CAP CER AXIAL .01 uF +80%-20% 25V C1,2,6,7		RP P 1 P C P EA	4	C93928	Jul-81	
097	8 130-0003	1B CAP CER AXIAL .1 uF +80%-20% 25V C13,C14		RP P 1 P C P EA	2	C939		14-Apr-83
028	8 130-0007	1B CAP CER AXIAL .1 uF +80%-20% 25V C3-5,10-16,21,22,25, C27,35-37,42-45,47 C48-51,53,55-57,63		RP P 1 C P EA	31	C93901	Mar-82	
031	8 130-0200	1A CAP CER .001 uF 10% 25V C24, C32		RP P 1 C P EA	2	C59928	Jul-81	
030	8 130-0201	1A CAP CER .0022 uF 10% 25V C19,23,28-31,26,62		RP P 1 C P EA	8	C59928	Jul-81	
036	8 137-5401	1A CAP DIP MICA 20 PF 5% 500V C61		RP P 1 C P EA	1	C54128	Jul-81	
035	8 137-5701	1A CAP DIP MICA 47 PF 5% 500V C34		RP P 1 P C P EA	1	C54128	Jul-81	
034	8 137-5801	1A CAP DIP MICA 75 PF 5% 500V C8		RP P 1 C P EA	1	C54128	Jul-81	
032	8 137-6101	1A CAP DIP MICA 100 PF 5% 500V C33		RP P 1 P C P EA	1	C54128	Jul-81	
033	8 137-6301	1A CAP DIP MICA 150 PF 5% 500V C7, C18, C17, C20		RP P 1 C P EA	4	C54128	Jul-81	
037	8 151-4701	1C INDUCTIVE, 5.6 OHM 10%		RP P 1 * P EA	1	C19528	Jul-81	

EFFECTIVITY DATE: ALL

INDEPENDENT BILLS OF MATERIAL

PARENT PART: A9M0005

FG PROFILE, "GENERIC" DRIVE - USA  
ERC: A SRCE CODE: B TYPE: 1

UM: FA PROD CODE: DH  
ABC: \* PLAN CODE: F

ECN: F354 ASSEMBLY QTY: 1  
DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR ST S A P	EXTENDED	ECN	START	DATE	CHG	S/N	DATE	CLOSE	S/N
		REMARKS	CD C Y P R I U M	QTY PFR								
021	8 156-0100	A DELAY LINE 14 PIN DIF 100 OHM, 50 KPF 1 * P E 0		1	792	28-Jul-81						
022	8 156-0110	A DELAY LINE 14 PIN DIF 500 OHM 100 KPF 1 * P E A		1	792	28-Jul-81						
007	8 301-0045	A IC, 7445 U4	RI P 1 C P E A	1	C06328	28-Jul-81						
001	8 301-0074	A IC, 7474 U2	RI P 1 P C P E A	1	C06328	28-Jul-81						
005	8 305-0014	A IC, 74LS14 U30	RI P 1 P R P E 0	1	442	28-Jul-81						
002	8 305-0174	A IC, 74LS174 U29	RI P 1 P B P E A	1	442	28-Jul-81						
004	8 307-0064	A IC, 74S64 U27	RI P 1 B P E A	1	C06328	28-Jul-81						
013	8 325-0102	A QUAD 2-INPUT NOR GATE U18	RI P 1 C P E A	1	741	28-Jul-81						
010	8 325-0107	A TRIPLE 2-INPT EXCL OR/EXCL NOR GA RI P 1 C P E A		2	741	28-Jul-81						
008	8 325-0114	A TRIPLE LINE RECEIVER U5, U14	RI P 1 C P E A	2	741	28-Jul-81						
009	8 325-0116	A TRIPLE LINE RECEIVER U26, U9	RI P 1 C P E A	2	741	28-Jul-81						
012	8 325-0117	A DL-2-WID 2-3-INPT OR-AND/OR-AND-I RI P 1 C P E A		1	741	28-Jul-81						
011	8 325-0131	B IC ECL HIGH SPEED DUAL D FLIP-FLO RI P 1 C P E A		6	C25528	28-Jul-81						
006	8 327-0453	A IC, DUAL PERIPHERAL DRIVES U11,17,19,20,21,22	RI P 1 * P E A	1	757	28-Jul-81						
096	8 335-0007	A PROG HEX 16 INPT REG AND-OR GT AR KL P 1 P B P E A		1	642	28-Jul-81						
003	8 341-0069	A MFM PAL PROG HEX 16 INPT REG AND-OR GT AR KL P 1 * P E A		1	F10501	28-Mar-82						
014	8 351-2907	A IC TRANS ARRAY QUAD FMP GEN PURFO RP P 1 C P E A		3	750	28-Jul-81						
016	8 351-3127	A TRANSISTOR, ARRAY NFN HIGH FREQ. U31, U23, U12	RP P 1 C P E A	1	750	28-Jul-81						
023	8 351-6700	A IC, TRANS, ARRAY QUAD COMP. PAIRS RI P 1 C P E A		2	750	28-Jul-81						
058	8 353-0005	A IC REG, +5V 100MA TO 92, 3 TERMNL RI P 1 C P E A		1	792	28-Jul-81						
018	8 353-0319	A IC, HIGH SPEED DUAL COMPARTOR RI P 1 C P E A		1	750	28-Jul-81						
017	8 353-0353	A DUAL FET OP AMP/BUFFER U25, U8	RP P 1 C P E A	2	750	28-Jul-81						
015	8 353 0592	A IC, VIDEO AMPLIFIER U6	RI P 1 C P E A	1	750	28-Jul-81						
024	8 371-4152	10 DIODE FAST SWITCH IN4148 500MW 30 PPF 1 C P E A		27	C53828	28-Jul-81						

INFINITE BILLS OF MATERIAL

PARENT PART: A9M0005 1 FG, PROFILE, 'GENERIC' DRIVE - USA UM: EA PROD CODE: DH ECN: F354 ASSEMBLY QTY: 1  
 ERC: A SRCE CODE: C TYPE: 1 ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	PR ST	UM	EXTENDED QTY PER	ECN	START DATE	CLOSE DATE	S/N
100	8	372-2222	1A	TRANS,NFN,SWITCHING AND AMP 2N222 ALT P/N FOR ITEM 23	** * * EA	0	C40308-Jul-83		
101	8	372-2907	A	XSTR:2N2907, PNP SWITCH & AMPLIFI U1-QTY 2 ALT P/N FOR ITEM 23	** * * EA	0	C25908-Jul-83		
102	8	372-3904	A	TRANSISTOR,NFN SW,8AMP, 2N3904 ALT P/N FOR ITEM 23	RP P 1 P C P EA	0	C30308-Jul-83		
103	8	372-3906	1B	TRANSISTOR,PNP SW,8AMP, 2N3906 U24-QTY 2 ALT P/N FOR ITEM 23	RP P 1 P C P EA	0	C76808-Jul-83		
026	8	375-0010	1A	DIODE REFERENCE 10ma 1.2V CR15	RP P 1 C P EA	1	C53828-Jul-81		
019	8	375-0012	1A	DIODE DUAL VOLT VAR CAP 200ma 32V Q2	RP P 1 * P EA	1	C53828-Jul-81		
020	8	376-0016	A	FET, N-CHANNEL VOLT CONTRL RESIS. Q1	RP P 1 * P EA	1	C30328-Jul-81		
090	8	511-0801	C	SOCKET, IC 8 PIN	RP P 1 P C P EA	3	799 28-Jul-81	14-Apr-83	
091	8	511-1401	C	SOCKET, IC 14 PIN	RP P 1 P C P EA	12	799 28-Jul-81	14-Apr-83	
092	8	511-1601	C	SOCKET, IC 16 PIN	RP P 1 P C P EA	17	799 28-Jul-81	14-Apr-83	
093	8	511-2001	C	SOCKET, IC 20 PIN	RP P 1 P C P EA	1	799 28-Jul-81	14-Apr-83	
087	8	515-0120	1B	CONN,HDR,SGL ROW,4P	RP P 1 P C P EA	15	C78128-Jul-81		
085	8	515-0130	1B	CONN,HDR,RT ANG,DBL ROW,8/16P J5	RP P 1 * P EA	1	C78128-Jul-81	02-Mar-82	
088	8	515-0131	1B	CONN,HDR,RT ANG,DBL ROW,17/34P J2	RP P 1 C P EA	1	C78101-Mar-82	28-Aug-83	
086	8	515-0140	1A	CONN,HDR,RT ANG,5P,W/LKG RAMP J6-8	RP P 1 * P EA	3	C78128-Jul-81		
105	8	515-0380	1A	CONN,HDR,RT ANG,DBL ROW,17/34P J2	** * * EA	1	C78129-Aug-83		
104	8	550-0101	1C	TUBING, HEAT SHRINK 1/4 ID BLACK USE W/ALT P/N 100-101 ON U1	EX X 7 P C P FT	0	C50308-Jul-83		
095	8	820-0054	AE	PCB, ANALOG PROFILE	RP P 1 * P EA	1	P21401-Mar-82		
001	6	699-0054	A	ASSY, O.E.M. HEAD DISC (H.D.A.)	VX A 1 P A P EA	1	600 14-Dec-82		
005	4	699-5011	1B	PURCH ASSY,COATD TOP CVR,PRFLE-B	** * * EA	1	L05112-Dec-83	05-Jan-84	
001	5	815-5007	1C	COVER, TOP, PROFILE	RM P 1 * P EA	1	F40812-Dec-83		
006	4	810-0090	1A	DRESS PANEL, DRIVE, PROFILE	RM P 1 * P EA	1	P56712-Dec-83		
007	4	810-0091	1B	DRESS PANEL, FWR SPLY PROFILE	RM P 1 * P EA	1	F64412-Dec-83		
012	4	825-0207	1B	LABEL, FCC NON COMPLIANCE APPL 3	EX X 7 P C P EA	1	P59312-Dec-83	05-Jan-84	
014	4	835-0172	A	MUT, U TYPE .017 THK	** * * EA	1	C67812-Dec-83		
009	5	430-1012	1C	SCF TAP 6-32X.312 FN CRS REC STL	X * * P EA	4	C54623-May-83		
021	3	825-0113	1B	LABEL,CAUTION PROFILE/DUOFILE	EX P 7 * P EA	1	F4115-Mar-84		
011	3	825-0114	1E	LABEL, PROFILE MOUFL & SERIAL NO.	EX P 7 * P EA	1	F63115-Mar-83		
008	3	825-0116	C	LABEL, INDIVIDUAL CARTON PROFILE	EX P 7 * P EA	1	F23415-Mar-83		
009	7	825-0209	B	LABEL, FCC NON COMPLIANT APPL 3	EX X 7 P C P EA	1	P59315-Mar-83	14-Sep-83	

EFFECTIVITY DATE: 01

INDENTED BILL OF MATERIAL

PARENT PART: A9M0005

ECN: F354 ASSEMBLY NTY: 1  
DATE: 15-Mar-83

FG, PROFILE, "GENERIC" DRIVE USA UM: EA  
SRC: A SRC CODE: G TYPE: I

PROD CODE: DH  
PLAN CODE: F

ITEM	LEVEL	COMPONENT PART NUMBER	PART DESCRIPTION	REMARKS	UNIT	QTY	UNIT	EXTENDED QTY	CHG	DATE	STAR	S/N	CLOS	S/N
026	3	825-0311	1B LABEL, LOGO 16MM BY 16MM		EA	1	EA	1	F51415	Mar-83				
027	3	825-0313	1B LABEL, NAMEPLATE, PROFILE		EA	1	EA	1	F51415	Mar-83				
028	3	825-0315	1C LABEL, LED PROFILE		EA	1	EA	1	F51415	Mar-83				
010	3	825-0317	A LABEL, FRAGILE, PROFILE		EA	4	EA	4	F11201	Jun-83				
014	3	825-0328	A LABEL, DO NOT REMOVE END CAPS		EA	2	EA	2	F12515	Mar-83				
015	3	825-0329	A LABEL, SERIAL NUMBER		EA	0.6000	EA	0.6000	F12415	Mar-83				
017	3	918-0050	B ANGLE BOARD, PALLETIZING, 2X2X36		EA	0.3330	EA	0.3330	M58315	Mar-83				
018	3	918-0051	B SEALS, STRAPPING, 50 DY		EA	0.3330	EA	0.3330	M58315	Mar-83				
019	3	918-0052	R TAFF, STRAPPING, CONTRAX 816		EA	0.0007	EA	0.0007	M58315	Mar-83				
020	3	918-0071	R PALLET, 48 X 40 2 WAY ENTRY		EA	0.1670	EA	0.1670	M72515	Mar-83				
016	3	919-0010	A LABEL, MODEL TYPE "US STD" RUBBER STAMP OR PEN		EA	1.3330	EA	1.3330	F33015	Mar-83				
031	3	942-0115	A BAG, BUBBLE 8 X 6		EA	1	EA	1	F11330	Jun-83				30-Sep-83
012	3	942-0117	1C BOX, 29.5 X 21.25 X 16.13, PROFIL		EA	1	EA	1	F39915	Mar-83				06-Jul-83
022	3	942-0142	A BOX, OFF 19.25 X 10.75 X 6.88		EA	1	EA	1	F12515	Mar-83				06-Jul-83
025	3	944-0091	1A CUSHION BLOCK, EPS, PROFILE (TO REPLACE ACC KIT)		EA	1	EA	1	F35415	Mar-83				06-Jul-83
009	3	946-0003	B TAPE, P.S. 2 inch X 60 yard ALT FOR ITEM 24		EA	0	EA	0	C06415	Mar-83				
024	3	946-0010	A TAPE, SEALING GLASS WEB #341 ALT QTY .0150		EA	0.0100	EA	0.0100	883 15	Mar-83				
023	3	946-0011	A TAPE, PRESSURE SENSITIVE 2 INCH, AU ALT FOR ITEM 24		EA	0	EA	0	C04915	Mar-83				
007	3	946-0012	1C STRAPPING, POLYPRO 1/2 INCH ALT QTY .0009		EA	0.0010	EA	0.0010	F72215	Mar-83				

EFFECTIVE DATE: ALL  
 PARENT PART: APM1005  
 FG, PROFILE "GENERIC" DRIVE - EURO UM: EA PROD CODE: 0H ECN: P354 ASSEMBLY QTY: 1  
 ERG: A SRCF CODE: 0 TYPE: 1 ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	PRESTIGAP	UN	EXTENDED	QTY	FF	ECN	DATE	START DATE	S/N	CLOSE DATE	S/N
001 2	656-8204	1H FG, PROFILE "GENERIC" DRIVE-EURO		* * * * *	EA		1		L30515	Mar-83				
003 3	030-0183	1C REGIS. CARD, PERIPH. & SOFTWARE		EX X 7 F C P EA			1		A92215	Mar-83			11-Dec-83	
002 3	030-0273	1D UNPACKING INSTRUCTIONS, PROFILE		EX X 7 C P EA			1		F7915	Mar-83				
001 3	030-0665	1C PACK LIST, PROFILE DRIVE - EURO		* * * * *	EA		1		F67515	Mar-83				
005 3	600-2515	A ASSY, END PAD		WS A 1 * T EA			2		F12515	Mar-83			06-Jul-83	
013 3	600-2516	B ASSY, END CAP, PROFILE		WS A 1 * P EA			2		F56815	Mar-83			06-Jul-83	
006 3	600-2517	A ASSY., TOP/BOTTOM PAD, PROFILE		* * * * *	EA		2		F26515	Mar-83			06-Jul-83	
030 3	602-0041	1B ASSY, SHIPPING CTN - PROFILE FG'S		* * * * *	EA		1		L26707	Jul-83				
001 4	600-2515	A ASSY, END PAD		WS A 1 * P EA			2		F12507	Jul-83				
004 4	600-2516	B ASSY, END CAP, PROFILE		WS A 1 * P EA			2		F56807	Jul-83				
002 4	600-2517	A ASSY., TOP/BOTTOM PAD, PROFILE		* * * * *	EA		2		F26507	Jul-83				
003 4	942-0117	1C BOX, 29.5 X 21.25 X 16.13, PROFIL		EX X 7 C P EA			1		F39907	Jul-83				
005 4	942-0142	A BOX, OFF 19.25 X 10.75 X 6.88		EX P 7 * P EA			1		P12507	Jul-83				
007 4	944-0091	1A CUSHION BLOCK, EPS, PROFILE (TO REPLACE ACC KIT)		* * * * *	EA		1		P35407	Jul-83				
006 4	946-0010	A TAPE, SEALING GLASS WEB #341		EX X 7 B P RI			0.0100		883 07	Jul-83				
031 3	656-6110	3E INACT.MFG.ASSY, CHASSIS, PROFILE		* * * * *	EA		0		L305				11-Dec-83	
003 4	400-1604	1C SCR 6-32X1/4 FN HD CRS REC STL ZN		EX X 7 C P EA			0		C54014	Dec-82			30-Aug-83	
008 4	400-1606	1C SCR 6-32X3/8 FN HD CRS REC STL ZN		EX X 1 F C P EA			0		C54001	Jun-83			30-Aug-83	
004 4	400-1608	1C SCR 6-32X1/2 FN HD CRS REC STL ZN		EX X 7 C P EA			0		C54014	Dec-82			31-May-83	
013 4	403-1606	1C SCR 6-32X3/8 FN CRS REC STL RL ZI		EX X 7 S C U EA			0		C54031	Aug-83				
009 4	430-1001	1C SCR TAP 8-18X.437 FN CRS STL ZN		EX X 7 P C P EA			0		C54014	Dec-82			14-Apr-83	
011 4	590-0046	1B CABLE, ASSY, I/O PROFILE		RC P 1 * P EA			0		P60314	Dec-82				
001 5	519-0110	1A CONN, D., IDC, 25P, W/O SR		RP P 1 * U EA			0		C78131	Aug-81				
002 5	589-0203	1B CABLE, FLAT 25 CONDUCTOR		* * * * *	FT		0		C52301	Oct-83				
003 5	590-0052	3A IDENTIFY SEE 569-0203		RC P 1 * P FT			0		C52331	Aug-81			30-Sep-83	
010 4	656-4103	A ASSY, PCR TSTD, I/O PROFILE A3		WT A 1 * P EA			0		F11314	Dec-82			14-Apr-83	
001 5	656-0103	1F ASSY, PCB UNTSTD, I/O PROFILE, A3		WU A 1 * P EA			0		F78131	Aug-81				
000 6	050-5007	1B SCHEMATIC, I/O CARD, PROFILE		D D 7 * U EA			0		P65104	Jan-82				
015 6	101-4103	1A RES 10K OHM 1/4W 5% R4,5,7		RP P 1 P C P EA			0		C67531	Jul-81				
014 6	101-4332	1A RES 3.3K OHM 1/4W 5% R1,3,6		RP P 1 P C P EA			0		C67531	Jul-81				
029 6	101-4751	1A RES 750 OHM 1/4W 5% R2		RP P 1 C P EA			0		C67513	Nov-81				
034 6	112-0102	1B RES ARRAY 8 X 47 OHM 10% B1		RP P 1 F C P EA			0		C67531	Aug-81			12-Nov-81	
021 6	112-0104	1B RES ARRAY 7 X 470 OHM 5% B1		RP P 1 * P EA			0		C67531	Jul-81				
013 6	112-0105	1B RES ARRAY 8 X 330 OHM A7,8,7		RP P 1 * P EA			0		C67513	Nov-81			06-Nov-83	
036 6	112-0107	1B RES ARRAY 8 X 100 OHM A7,8,7		* * * * *	EA		0		C67507	Nov-83				
035 6	130-0003	1B CAP CER AXIAL .1 UF +80%-20% 25V		RP P 1 F C P EA			0		C93913	Nov-81			17-May-82	
016 6	130-0007	1B CAP CER AXIAL .1 UF +80%-20% 25V C1-C17		RP P 1 C P EA			0		C93918	May-82				
032 6	152-6101	1A CAP CER 100 P.F. 20% 50V C11		RP P 1 P C P EA			0		C54113	Nov-81				
031 6	158-6600	A BEAD, FERRITE I1		RP P 1 P C P EA			0		UC6213	Nov-81				
003 6	201-0030	A IC, 7430 I1		RP P 1 P C P EA			0		C02313	Nov-81				

UNIT: [Unit Name] | LOCATION: [Location] | DATE: [Date]

PROJECT: [Project Name] | TASK: [Task Name] | PLAN CODE: [Code]

ITEM	DESCRIPTION	QTY	UNIT	DATE	STATUS	REMARKS	DATE
008	A IC, 74LS259	6	IC	74LS259	0	RI P 1 P C P EA	066331 Jul-81
009	A IC, 74LS34	6	IC	74LS34	0	RI P 1 P C P EA	066331 Jul-81
004	A IC, 74LS10	6	IC	74LS10	0	RI P 1 P P P EA	442 31-Jul-81
002	A IC, 74LS14	6	IC	74LS14	0	RI P 1 P B P EA	442 31-Jul-81
033	A IC, 74LS38 QUAD 2 INPUT BUFFER	6	IC	74LS38	0	RI P 1 P B P EA	649 31-Aug-81
012	A IC, 74LS109	6	IC	74LS109	0	RI P 1 P B P EA	442 31-Jul-81
005	A IC, 74LS125	6	IC	74LS125	0	RI P 1 P B P EA	442 31-Jul-81
001	A IC, 74LS132	6	IC	74LS132	0	RI P 1 P B P EA	442 31-Jul-81
006	A IC, 74LS138	6	IC	74LS138	0	RI P 1 P B P EA	442 31-Jul-81
009	A IC, 74LS244	6	IC	74LS244	0	RI P 1 P B P EA	442 31-Jul-81
010	A IC, 74LS280 9-BIT PARITY	6	IC	74LS280	0	RI P 1 P B P EA	649 31-Jul-81
011	A IC, 74LS368	6	IC	74LS368	0	RI P 1 P B P EA	442 31-Jul-81
008	A IC, 74LS374	6	IC	74LS374	0	RI P 1 P B P EA	442 31-Jul-81
026	IC SCR 4-40X3/8 FN HD CRS REC STL ZN	6	IC	4-40X3/8	0	EX X 7 P C P EA	C54031-Jul-81
022	C SOCKET, IC 14 PIN	6	Socket	IC 14 PIN	0	RF P 1 P C P EA	799 31-Jul-81
023	C SOCKET, IC 16 PIN	6	Socket	IC 16 PIN	0	RF P 1 P C P EA	799 31-Jul-81
024	C SOCKET, IC 20 PIN	6	Socket	IC 20 PIN	0	RF P 1 P C P EA	799 31-Jul-81
025	1E CONN, PIN, SINGLE	6	Conn	PIN, SINGLE	0	RF P 1 P C P EA	C78131-Jul-81
030	1E CONN, FC TAIL, 90 DEG, MET, LNC FTFR	6	Conn	FC TAIL, 90 DEG, MET, LNC FTFR	0	RF P 1 * P EA	C78113-Nov-81
018	1A CONN, PLUG, CONTACT KEY, 0, SUB	6	Conn	PLUG, CONTACT KEY, 0, SUB	0	RF P 1 C P EA	C78131-Jul-81
020	AC PCB 1/0, PROFILE, FOR A2	6	PCB	PROFILE, FOR A2	0	EM P 1 * P EA	P13531-Jul-81
027	A NUT/WASHER ASSY, (PEPS) 4-40	6	Assy	NUT/WASHER ASSY, (PEPS) 4-40	0	EX P 7 * P EA	834 31-Jul-81
002	3D INACT, MFG SUBASSY, BASE, PROFILE	4	Subassy	MFG SUBASSY, BASE, PROFILE	0	** * * EA	L30514-Dec-82
005	IC SCR 6-32X1/4 FN HD CFS REC STL ZN	5	IC	6-32X1/4 FN HD CFS REC STL ZN	0	EX X 7 C P EA	C54014-Dec-82
006	IC SCR 6-32X3/8 FN HD CFS REC STL ZN	5	IC	6-32X3/8 FN HD CFS REC STL ZN	0	EX X 1 P C P EA	C54001-Apr-83
011	1E CONN, PIN, SINGLE	6	Conn	PIN, SINGLE	0	RF P 1 P C P EA	C54001-Apr-83
007	1E CONN, PIN, SINGLE	6	Conn	PIN, SINGLE	0	RF P 1 P C P EA	C54001-Apr-83
004	1E CONN, PIN, SINGLE	6	Conn	PIN, SINGLE	0	RF P 1 P C P EA	C54001-Apr-83
001	1E CONN, PIN, SINGLE	6	Conn	PIN, SINGLE	0	RF P 1 P C P EA	C54001-Apr-83
003	1E CONN, PIN, SINGLE	6	Conn	PIN, SINGLE	0	RF P 1 P C P EA	C54001-Apr-83

31-May-83

20-Jun-83





EFFECTIVE DATE: 01-01-83

PARENT PART: ANALOGS  
 F0: PROFILE 'GENERIC' DEVICE - FURN  
 UM: F0  
 PROD CODE: DM  
 ECH: F-54  
 ASSEMBLY QTY: 1  
 SRC: A  
 SRC CODE: G  
 TYPE: 1  
 ABC: \*  
 PLAN CODE: P  
 DATE: 15-Mar-83

ITEM NUMBER	COMPONENT PART NUMBER	DESCRIPTION	QTY	UNIT	EXTENDED PLAN CODE	START DATE	END DATE
039	8 101-4392	1A RES 3.9K OHM 1/4W 5% R14	0	PCP EA	0	14-Oct-83	
041	8 101-4510	1A RES 51 OHM 1/4W 5% R16	0	PCP EA	0	14-Oct-83	
077	8 101-4512	1A RES 5.1K OHM 1/4W 5% R22	0	PCP EA	0	14-Oct-83	
035	8 111-0021	1A RES NETWORK 7 X 2K OHM 5% RF1	0	PCP EA	0	14-Oct-83	
034	8 111-0022	1A RES NETWORK 7 X 10K OHM 5% RF2	0	PCP EA	0	14-Oct-83	
070	8 112-0102	1B RES ARRAY 8 X 47 OHM 10% U1,U2	0	PCP EA	0	12-Nov-81	
001	8 112-0105	1B RES ARRAY 8 X 330 OHM U1,U2	0	* P EA	0	06-Nov-83	
081	8 112-0107	1B RES ARRAY 8 X 100 OHM U1,U2	0	* * EA	0		
043	8 125-5701	1B CAP ELECT 47 uF -10%175% 10V C8,C21,C29,C30	0	PCP EA	0		
045	8 130-0007	1B CAP CER AXIAL .1 uF +80%-20% 25V A CRYSTAL, 10MHz	0	PCP EA	0		
032	8 197-0017	1A CLOCK OSC,CRYSTAL 10 MHz (TTL)	0	* P EA	0	14-Oct-83	
078	8 197-0502	1A CLOCK OSCILLATOR,CRYSTAL,10 MHz	0	* * EA	0		
080	8 197-0504	1A CLOCK OSCILLATOR,CRYSTAL,10 MHz ALT FOR ITEM 78	0	* * EA	0		
029	8 301-0006	A IC, 7406 U41	0	* P EA	0		
009	8 305-0000	A IC, 74LS00N U15,U26	0	P B P EA	0		
026	8 305-0002	A IC, 74LS02N U31	0	P B P EA	0		
025	8 305-0008	A IC, 74LS08 U32	0	P B P EA	0		
017	8 305-0014	A IC, 74LS14 U23	0	P B P EA	0		
027	8 305-0038	A IC, 74LS38 QUAD 2 INPUT BUFFER U24	0	P B P EA	0		
019	8 305-0109	A IC, 74LS109 U36	0	P B P EA	0		
014	8 305-0153	A IC, 74LS153 U6	0	P B P EA	0		
006	8 305-0161	A IC, 74LS161 U10,U16,U17	0	P B P EA	0		
020	8 305-0163	A IC, 74LS163 U22	0	P B P EA	0		
017	8 305-0174	A IC, 74LS174 U30,U34,U38	0	P B P EA	0		
014	8 305-0140	A IC, 74LS240 U7	0	P B P EA	0		
002	8 305-0144	A IC, 74LS244 U11,U12	0	P B P EA	0		

COMPONENT PARTS OF MOTOR

PARENT PART: A9M1005 PARENT PART: 49M1005 PARENT PART: 49M1005  
 FCN: P334 ASSEMBLY QTY: 1  
 DATE: 15-MAR-83

ITEM	ITEM	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	REP	QTY	UNIT	EXTENDED	DATE	QTY	DATE
010	R	305-0257	A IC, 74LS257		RI	1	P B P EA	0	442	31	AUG-81
030	B	305-0280	A IC, 74LS280	9 HIT PAFITY	RI	1	P B P EA	0	649	31	AUG-81
015	B	305-0323	A IC, 74LS323		RI	1	P B P EA	0	442	31	AUG-81
047	B	305-0377	A IC, 74LS377		RI	1	P B P EA	0	442	31	AUG-81
024	B	307-0074	A IC, 74S74		RI	1	P B P EA	0	C06331		AUG-81
011	B	307-0086	A IC, 74S86		RI	1	P B P EA	0	C06331		AUG-81
008	B	334-2114	1C IC 1024x4 STATIC RAM 2114 TST&BRN	U11,U18	RI	1	F C P EA	0	C62131		AUG-81
000	9	062-0083	1B SPEC, 2114 RAM BURN-IN		EX	D 7	* U EA	0	C31415		JUL-83
001	9	333-2114	1B IC 1024 X 4 STATIC RAM 2114		RL	P 1	C P EA	0	C4715		JUL-83
073	B	335-0004	A PROM, 512 X 8 (UNPROGRAMMED)		RL	P 1	F C P EA	0	C02131		AUG-81
071	B	335-0006	A PROM, 1024 X 8 (UNPROGRAMMED)		RL	P 1	F C P EA	0	642	31	AUG-81
072	B	335-6309	A PROM, MMI 6309-1		RL	P 1	F C P EA	0	C-6	31	AUG-81
012	B	337-8253	MA PROGRAMMABLE INTERVAL TIMER		RL	P 1	F A P EA	0	642	31	AUG-81
004	B	337-8603	B IC SOCKET MICROPRO. W/24P FIGGYBA		RL	P 1	* P EA	0	C14831		AUG-81
018	B	337-9401	A CRC GENERATOR/CHECKER		RL	P 1	P A P EA	0	642	31	AUG-81
021	B	341-0066	A PROM, U29		RL	A 1	* P EA	0	F10513		NOV-81
022	B	341-0067	A PROM, U37		RL	A 1	* P EA	0	F10513		NOV-81
007	B	341-0068	A RAMPAL		RL	P 1	* P EA	0	F10513		NOV-81
031	B	341-0080	B PROM FROM 2K PROFILE CONTROLLER		RL	P 1	* P EA	0	F18413		NOV-81
074	B	341-0129	A EPROM-FIRMWARE 3.90 78 PROFILE-27		RL	A 1	* P EA	0	F11031		AUG-81
001	9	335-2716	A EPROM, 2048 X 8 2716		RL	P 1	F C P EA	0	642	31	AUG-81
028	B	351-2074	A QUAD DARLINGTON XSTR ARRAY 2074R		RP	F 1	P B P EA	0	642	31	AUG-81
023	B	359-4024	A VOLTAGE CONTROLLED MULTIVIBRATOR		RI	P 1	P B P EA	0	642	31	AUG-81
033	B	371-4001	1A DIODE RECTIFIER 1N4001 1.0A 50V		RP	F 1	P C P EA	0	C59931		AUG-81
076	B	371-4128	1A DIODE ZENER 1N4128 250mW 60V		RP	F 1	* P EA	0	C51831		AUG-81
064	B	371-4148	A DIODE FAST SWITCH 1N4148 200mA 75		RP	F 1	P C P EA	0	C53813		NOV-81
062	B	400-1406	1C SCR 4-40X3/8 FH HD CRS REC STL ZN		EX	X 7	F C P EA	0	C54031		AUG-81
005	B	511-1401	1C SOCKET, 10 14 PIN		RP	F 1	P C P EA	0	799	07	AUG-82
006	B	511-1401	1C SOCKET, 10 14 PIN		RP	F 1	P C P EA	0	799	31	AUG-81
007	B	511-1401	1C SOCKET, 10 14 PIN		RP	F 1	P C P EA	0	799	31	AUG-81
008	B	511-2001	1C SOCKET, 10 20 PIN		RP	F 1	P C P EA	0	799	31	AUG-81
009	B	511-2301	1C SOCKET, 10 23 PIN		RP	F 1	P C P EA	0	799	31	AUG-81
010	B	511-2301	1C SOCKET, 10 23 PIN		RP	F 1	P C P EA	0	799	31	AUG-81

RECEIVED BY: [Name] DATE: [Date]

COMPONENT PART NUMBER: 09M1005  
PART DESCRIPTION: DRIVE SHAFT  
EQUIP: F-154 ASSEMBLY QTY: 1  
DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	PART DESCRIPTION	FRS	TS	DP	UM	FA	PROD CODE: DH	EXTENDED QTY PER	ECR P/N	START DATE	S/N	CLOSE DATE	SUB
061	8	515-0005	1B CONN, PIN, SINGLE	RP	P	1	P	C	P	EA	0	C78131	Aug-81		
054	8	515-0053	1C CONN, HDR, STR, 2P	RP	P	1	P	C	P	EA	0	C78131	Aug-81		
053	8	515-0083	1A HEADER, JO PIN RT ANGLE W/O EARS	RP	P	1	C	P	EA	0	0	C48031	Aug-81	16-Nov-82	
066	8	515-0150	1A CONN, HDR, RT ANG, 5P, .156 CTR, W/LKG RAMP	RP	P	1	*	P	EA	0	0	C78113	Nov-81		
067	8	515-0160	1A CONN, HDR, RT ANG, 2P, W/LKG RAMP	RP	P	1	*	P	EA	0	0	C78113	Nov-81		
065	8	519-0100	1B CONN, FC TAIL, 90 DEG, MET, LNC FT/PRI	RP	P	1	*	P	EA	0	0	C78113	Nov-81		
049	8	520-0011	1A CONN, PLUG, CONTACT KEY, "D" SUB	RP	P	1	C	P	EA	0	0	C78131	Aug-81		
079	8	570-2239	1A WIRE, STRANDED 22 AWG, GREEN, BULK	*	*	*	*	*	FT	0	0	C50915	Oct-83		
068	8	571-0001	A WIRF, BUS BAR, 20 AWG, .5 IN.	EX	X	7	*	U	FT	0	0	F23213	Nov-81	14-Oct-83	
046	8	820-0055	1D FCR, CONTROLLER, PROFILE	RP	P	1	*	P	EA	0	0	F17631	Aug-81		
069	8	835-0150	A NUT/WASHER ASSY, (KFFS) 4-40	EX	F	7	*	P	EA	0	0	834	13-Nov-81		
001	6	699-0059	AB PURCH. ASSY, POWER SUPPLY PROFILE	UX	P	1	A	P	EA	0	0	F18114	Dec-82		
005	6	825-0320	A LABEL, WARNING PWR SUP PROFILE	EX	P	7	C	P	EA	0	0	F10914	Dec-82		
002	6	860-0200	1C STANDOFF, FLASTIC .188"	EX	P	7	C	P	EA	0	0	C52014	Dec-82		
011	6	860-0210	MA STANDOFF, HEX 6-32 X 1/4	EX	P	7	*	P	EA	0	0	F109		06-Apr-83	
003	6	860-0213	1A STANDOFF, 6-32, 5/16", METAL JACKNUT	EX	X	7	S	C	EA	0	0	C32530	Mar-83	16-Aug-83	
008	6	918-0023	0 1/4" TAN DOT	EX	X	7	S	C	EA	0	0		14-Dec-82		
004	6	918-0025	ALTN P/N FOR ITEM 4 ALTN QTY 1	EX	X	7	S	C	EA	0	0		14-Dec-82		
009	6	918-0029	0 1/4" RED DOT ALTN P/N 918-0023 ALTN P/N 918-0029 ALTN P/N 918-0031	EX	X	7	S	C	EA	0	0		14-Dec-82		
010	6	918-0031	0 1/4" ORANGE DOT ALTN P/N FOR ITEM 4 ALTN QTY 1	EX	X	7	S	C	EA	0	0		14-Dec-82		
002	5	656-5140	3R INACT, MFG, SUBASSY, H.D.A., PROFILE ALTN QTY 1	EX	X	7	S	C	EA	0	0		14-Dec-82		
005	6	400-1604	1C SCR 6-32X1/4 PN HD CRS REC STL ZN	EX	X	7	C	P	EA	0	0	L30514	Dec-82		
004	6	590-0048	1B CABLE, ASSY, CNTRLR TO ANALOG FCR	RP	P	1	*	P	EA	0	0	C54014	Dec-82		
001	7	513-0020	1R CONN, CD EDG, INC, 17/34P, W/O EAR	RP	P	1	C	U	EA	0	0	F60314	Dec-82		
002	7	517-0035	1E CONN, SRT, INSUL. DISPL., 17/34P	RP	P	1	C	U	EA	0	0	C78131	Aug-81		
003	7	569-0204	1R CABLE, FLAT 34 CONDUCTOR	RP	P	1	C	U	EA	0	0	C78131	Aug-81		
004	7	590-0053	3A IDENTIFY SEE 569-0204	RP	P	1	*	P	EA	0	0	C52301	Oct-83		
002	6	590-0105	A CABLE ASSY, #16 AWG GROUND WIRE	RC	P	1	*	P	EA	0	0	C523		30-Sep-83	
003	7	517-1102	1B TERMINAL, RING TONGUE #8	RP	P	1	*	P	EA	0	0	F18014	Dec-82		
002	7	517-1211	1C TERMINAL, RECEPT 4.75 Y .51 TOP	RP	P	1	*	P	EA	0	0	C34401	Mar-82		
001	7	520-1601	A WIRF, 16 AWG, CRAI, 26/30, 4.80"	UX	P	1	*	P	EA	0	0	C62801	Mar-82		
002	7	550-4101	A WIRF, 16 AWG, CRAI, 26/30, 4.80"	UX	P	1	*	P	EA	0	0	C62801	Mar-82		
001	7	550-4101	A WIRF, 16 AWG, CRAI, 26/30, 4.80"	UX	P	1	*	P	EA	0	0	F11114	Dec-82		
001	7	550-4101	A WIRF, 16 AWG, CRAI, 26/30, 4.80"	UX	P	1	*	P	EA	0	0	L05941	Aug-81		
001	7	550-4101	A WIRF, 16 AWG, CRAI, 26/30, 4.80"	UX	P	1	*	P	EA	0	0	F02701	Mar-82		
001	7	550-4101	A WIRF, 16 AWG, CRAI, 26/30, 4.80"	UX	P	1	*	P	EA	0	0	C62520	Jul-81		

IDENTIFIED BILLS OF MATERIAL

EFFECTIVITY DATE: ALL

PARENT PART: 49H1005

FG, PROFILE 'GENERIC' DRIVE - EURO UM: EA FRD CODE: DH ECN: P154 ASSEMBLY QTY: 1  
ERC: A SRCE CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	FRS T A F CD C Y P B I UM	EXTENDED QTY PFF	ECN CHG	START DATE	CLOSE DATE	S/N
051	8 101-4101	1A RES 100 OHM 1/4W 5Z	R101	RP P 1 P C P EA	0	C67528	Jul-81		
			R4,67						
053	8 101-4102	1A RES 1K OHM 1/4W 5Z	R2-3,R15,R20-21	RP P 1 P C P EA	0	C67528	Jul-81		
			R38-39,R48,R54,R59						
			R60-62,R85-88						
			R106,R108						
068	8 101-4103	1A RES 10K OHM 1/4W 5Z	R13,17,42-45,47	RP P 1 P C P EA	0	C67528	Jul-81		
			R49,70,81,117						
083	8 101-4104	1A RES 100K OHM 1/4W 5Z	R115	RP P 1 P C P EA	0	C67528	Jul-81		
080	8 101-4111	1A RES 110 OHM 1/4W 5Z	R91,92	RP P 1 P C P EA	0	C67528	Jul-81		
064	8 101-4121	1A RES 120 OHMS 1/4W 5Z	R25,26	RP P 1 P C P EA	0	C67528	Jul-81		
077	8 101-4122	1A RES 1.2K OHM 1/4W 5Z	R107	RP P 1 P C P EA	0	C67528	Jul-81		
075	8 101-4123	1A RES 12K OHM 1/4W 5Z	R73	RP P 1 P C P EA	0	C67528	Jul-81		
072	8 101-4151	1A RES 150 OHM 1/4W 5Z	R36,68,114	RP P 1 P C P EA	0	C67528	Jul-81		
061	8 101-4152	1A RES 1.5K OHM 1/4W 5Z	R7,82,83	RP P 1 P C P EA	0	C67528	Jul-81		
056	8 101-4182	1A RES 1.8K OHM 1/4W 5Z	R69	RP P 1 P C P EA	0	C67528	Jul-81		
081	8 101-4201	1A RES 200 OHM 1/4W 5Z	R110	RP P 1 P C P EA	0	C67528	Jul-81		
069	8 101-4203	1A RES 20.0K OHM 1/4W 5Z	R16,50	RP P 1 P C P EA	0	C76028	Jul-81		
062	8 101-4220	1A RES 22 OHM 1/4W 5Z	R23,24,32	RP P 1 P C P EA	0	C67528	Jul-81		
055	8 101-4241	1A RES 240 OHM 1/4W 5Z	R18,19	RP P 1 P C P EA	0	C67528	Jul-81		
079	8 101-4242	1A RES 2.4K OHM 1/4W 5Z	R80,40,41	RP P 1 P C P EA	0	C67528	Jul-81		
067	8 101-4243	1A RES 24K OHM 1/4W 5Z	R35	RP P 1 P C P EA	0	C67528	Jul-81		
066	8 101-4244	1A RES 240K OHM 1/4W 5Z	R31	RP P 1 P C P EA	0	C67528	Jul-81		
078	8 101-4272	1A RES 2.7K OHM 1/4W 5Z	R74	RP P 1 P C P EA	0	C67528	Jul-81		
082	8 101-4301	1A RES 300 OHM 1/4W 5Z	R111	RP P 1 P C P EA	0	C67528	Jul-81		
070	8 101-4331	1A RES 330 OHM 1/4W 5Z	R89,90	RP P 1 P C P EA	0	C67528	Jul-81		
073	8 101-4332	1A RES 3.3K OHM 1/4W 5Z	R100,76	RP P 1 P C P EA	0	C67528	Jul-81		
049	8 101-4300	1A RES 39 OHM 1/4W 5Z		RP P 1 P C P EA	0		Jul-81		

EFFECTIVITY DATE: ALL

PARENT PART: A9H1005

FG, PROFILE "GENERIC" DRIVE - EURO  
ERC: A SRCE CODE: G TYPE: 1

UM: EA FROM CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ARC: \* PLAN CODE: F DATE: 15-Mar-83

INDEXED BILLS OF MATERIAL

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR T S A P CD C Y P B L U M	EXTENDED QTY PER	ECN CHG	START DATE	CLOSE DATE
054	8 101-4391	1A RES 390 OHM 1/4W 5% R78,R112	RP P 1 P C P EA	0	C67528	Jul-81	
060	8 101-4392	1A RES 4.9K OHM 1/4W 5% R54 R9,R8,113,1,27 R118,119	RP P 1 P C P EA	0	C67513	Apr-83	
052	8 101-4471	1A RES 470 OHM 1/4W 5% R37,52-53,77	RP P 1 P C P EA	0	C67528	Jul-81	
084	8 101-4473	1A RES 47K OHM 1/4W 5% R116,71	RP P 1 P C P EA	0	C67528	Jul-81	
065	8 101-4511	1A RES 510 OHM 1/4W 5% R63,64,29,30,28	RP P 1 P C P EA	0	C67528	Jul-81	
071	8 101-4561	1A RES 560 OHM 1/4W 5% R99	RP P 1 P C P EA	0	C67528	Jul-81	
045	8 101-4681	1A RES 680 OHMS 1/4W 5% R11-12,R22	RP P 1 P C P EA	0	C67528	Jul-81	
074	8 101-4751	1A RES 750 OHM 1/4W 5% R75,79	RP P 1 C P EA	0	C67528	Jul-81	
063	8 101-4752	1A RES 7.5K OHM 1/4W 5% R5,6,33,34	RP P 1 P C P EA	0	C67528	Jul-81	
076	8 101-4822	1A RES 8.2K OHM 1/4W 5% R72	RP P 1 P C P EA	0	C67528	Jul-81	
057	8 101-4823	1A RES 82K OHM 1/4W 5% R46	RP P 1 C P EA	0	C67528	Jul-81	
048	8 108-1543	1A RES 1.54K OHM 1/4W 1% R84	RP P 1 C P EA	0	C75828	Jul-81	
042	8 108-1783	1A RES 1.78K OHM 1/4W 1% R10	RP P 1 C P EA	0	C75828	Jul-81	
041	8 108-1963	1A RES 1.96K OHM 1/4W 1% R105,104	RP P 1 * P EA	0	C75801	Mar-82	
047	8 108-3833	1A RES 3.83K OHM 1/4W 1% R93,R95-96,R97	RP P 1 * P EA	0	C75831	Jul-81	
039	8 108-3923	1A RES 3.92K OHM 1/4W 1% R65,66	RP P 1 P C P EA	0	C75828	Jul-81	
046	8 108-4531	1A RES 45.3 OHM 1/4W 1% R14	RP P 1 C P EA	0	C75828	Jul-81	
043	8 108-5623	1A RES 5.62K OHM 1/4W 1% R94,R98	RP P 1 C P EA	0	C75828	Jul-81	
106	8 109-0002	0 POT, TRIM 1K OHM 20%	RP P 1 P C P EA	0	442	10-Oct-83	
040	8 109-0005	A POT, TRIM 500 OHM, 20% ALIN P/N 109-0420	RP P 1 * P EA	0	C04518	May-82	09-Oct-83
098	8 109-0410	1A POT, 500 OHM 18 - 25 TURNS	RP P 1 C P EA	0	C50428	Jul-81	02-Mar-82
099	8 109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS ALIN P/N FOR ITEM 40	RP P 1 C P EA	0	F10518	May-82	09-Oct-83
073	8 111-0023	1A RES NETWORK 7 X 560 OHM 5% R92,8	RP P 1 C P EA	0	C67528	Jul-81	
094	8 111-0024	1A RES NETWORK 7 X 4.7K OHM 5% R92,1	RP P 1 C P EA	0	C67528	Jul-81	
095	8 111-0100	1P CAP TANT 4.7 uF 20% 100 R92,1	RP P 1 * P EA	0	C67528	Jul-81	

EFFECTIVITY DATE: ALL

INDEPENDENT RILLS OF MATERIAL

PARENT PART: A9M100S

FC: PROFILE "GENERIC" DRIVE - EURO UM: EA

PROD CODE: DH

FCN: F354 ASSEMBLY QTY: 1

REG: A SRCO CODE: G TYPE: 1 ARC: \*

DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	F PART DESCRIPTION	REMARKS	PR S T S A P	UM	EXTENDED QTY PER	FCN	START DATE	CLOSE DATE	S/N
037	8 127-0101	1R CAP TANT 10 UF 20% 15/16V	C38-C40	RP P 1	* P EA	0	C59928	Jul-81		
029	8 130-0002	1R CAP CER AXIAL .01 UF +80%-20% 25V	C1,2,5,7	RP P 1	P C P FA	0	C93928	Jul-81		
097	8 130-0003	1R CAP CER AXIAL .1 UF +80%-20% 25V	C13,C14	RP P 1	P C P EA	0	C939	14-Apr-83		
028	8 130-0007	1R CAP CER AXIAL .1 UF +80%-20% 25V	C3-5,10-16,21,22,25, 27,35-37,42-45,47	RP P 1	C P EA	0	C93901	Mar-82		
031	8 130-0200	1A CAP CER .001 UF 10% 25V	C48-51,53,55-57,63	RP P 1	C P EA	0	C59928	Jul-81		
030	8 130-0201	1A CAP CER .0022 UF 10% 25V	C24, C32	RP P 1	C P EA	0	C59928	Jul-81		
036	8 137-5401	1A CAP DIP MICA 20 PF 5% 500V	C19,23,28-31,26,62	RP P 1	C P EA	0	C54128	Jul-81		
035	8 137-5701	1A CAP DIP MICA 47 PF 5% 500V	C61	RP P 1	P C P EA	0	C54128	Jul-81		
034	8 137-5801	1A CAP DIP MICA 75 PF 5% 500V	C34	RP P 1	C P EA	0	C54128	Jul-81		
032	8 137-6101	1A CAP DIP MICA 100 PF 5% 500V	C8	RP P 1	P C P EA	0	C54128	Jul-81		
033	8 137-6301	1A CAP DIP MICA 150 PF 5% 500V	C33	RP P 1	C P EA	0	C54128	Jul-81		
027	8 151-4701	1C INDUCTOR, 5.6 OH 10%	C9, C18, C17, C20	RP P 1	* P EA	0	C39528	Jul-81		
021	8 156-0100	A DELAY LINE 14 PIN DIP 100 OHM, 50 DLY 2	L1, L2	RP P 1	* P EA	0	792 28	Jul-81		
022	8 156-0110	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1		RP P 1	* P EA	0	792 28	Jul-81		
007	8 301-0045	A IC, 7445	U4	RI P 1	C P EA	0	C06328	Jul-81		
001	8 301-0074	A IC, 7474	U2	RI P 1	P C P EA	0	C06328	Jul-81		
005	8 305-0014	A IC, 74LS14	U30	RI P 1	P B P EA	0	442 28	Jul-81		
002	8 305-0174	A IC, 74LS174	U29	RI P 1	P B P EA	0	442 28	Jul-81		
004	8 307-0064	A IC, 74S64	U27	RI P 1	B P EA	0	C06328	Jul-81		
013	8 325-0102	A QUAD 2-INPUT NOR GATE	U18	RI P 1	C P EA	0	741 28	Jul-81		
010	8 325-0107	A TRIPLE 2-INPT EXCL OR/EXCL NOR GA	U10, U15	RI P 1	C P EA	0	741 28	Jul-81		
008	8 325-0114	A TRIPLE LINE RECEIVER	U5, U14	RI P 1	C P EA	0	741 28	Jul-81		
009	8 325-0116	A TRIPLE LINE RECEIVER	U26, U9	RI P 1	C P EA	0	741 28	Jul-81		
012	8 325-0119	A DUAL 2-INPUT OR-AND/OR-AND-1	U15	RI P 1	C P EA	0	741 28	Jul-81		

INVENTORIES OF MATERIALS

PARENT PART: A9M1005  
EFFECTIVITY DATE: ALL  
FG, PROFILE 'GENERIC' DRIVE - EURO UM: EA PKOD CODE: IH FCN: F354 ASSEMBLY QTY: 1  
ERC: A SRCE CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FRSTSTAP	EXTEND	FCN	STAFF	CLOSE
			REMARKS	CDYFBT	UM	CHG	DATE	S/N
011	8	325-0131	IC ECL HIGH SPEED DUAL D FLIP-FLOP 1 C P EA U11,17,19,20,21,22		0	C25528	Jul-81	
006	8	327-0453	IC, DUAL PERIPHERAL DRIVES U3	RP 1	* P EA	757	28-Jul-81	
096	8	335-0007	PROG HEX 16 INFT REG AND-OR GT AR RL P 1 P B P EA	RL A 1	* P EA	642	28-Jul-81	02-Mar-82
003	8	341-0069	MEMFAL PROG HFX 16 INFT REG AND-OR GT ARY U28			F10501	Mar-82	
014	8	351-2907	IC TRANS ARRAY QUAD PNP GFN PURFO RP P 1 C P EA		0	750	28-Jul-81	
016	8	351-3127	TRANSISTOR, ARRAY NPN HIGH FREQ. U31, U23, U12	RP P 1	C P EA	750	28-Jul-81	
023	8	351-6700	IC, TRANS. ARRAY QUAD COMP. PAIRS RI P 1 C P EA U1, U24		0	750	28-Jul-81	
058	8	353-0005	ITEM 100-103 ALT P/N IC REG. +5V 100MA TO 92, 3 TERMNL RI P 1 C P EA		0	792	28-Jul-81	
018	8	353-0319	IC, HIGH SPEED DUAL COMPARATOR RG1	RI P 1	C P EA	750	28-Jul-81	
017	8	353-0353	DUAL FET OP AMP/BUFFER U13	RP P 1	C P EA	750	28-Jul-81	
015	8	353-0592	IC, VIDEO AMPLIFIER U25,U8	RI P 1	C P EA	750	28-Jul-81	
024	8	371-4152	DIODE FAST SWITCH 1N4152 500mW 30 RP P 1 C P EA U6 CR1-14, CR16-21, CR23-24, CR26		0	C53828	Jul-81	
100	8	372-2222	TRANS,NPN, SWITCHING AND AMP 2N222 ALT P/N FOR ITEM 23	**	** EA	C40308	Jul-83	
101	8	372-2907	XSTR, 2N2907, PNP SWITCH & AMPLIFI ALT P/N FOR ITEM 23	**	** EA	C25908	Jul-83	
102	8	372-3904	TRANSISTOR, NPN SW. & AMP. 2N3904 ALT P/N FOR ITEM 23	RP P 1	C P EA	C30308	Jul-83	
103	8	372-3906	TRANSISTOR, PNP SW. & AMP. 2N3906 ALT P/N FOR ITEM 23	RP P 1	C P EA	C76808	Jul-83	
026	8	375-0010	DIODE REFERENCE 10mA 1.2V CR15	RP P 1	C P EA	C53828	Jul-81	
019	8	375-0012	DIODE DUAL VOLT VAR CAP 200mA 32V RP P 1 * P EA U24-QTY 2 U24-QTY 2		0	C53828	Jul-81	
020	8	376-0014	FET, N-CHANNEL VOLT CONTRL RESIS. RP P 1 * P EA U2		0	C30328	Jul-81	
099	8	511-9891	SOCKET, IC 8 PIN U1	RP P 1	C P EA	750	28-Jul-81	14-Apr-83
097	8	511-1471	SOCKET, IC 14 PIN U2	RP P 1	C P EA	750	28-Jul-81	14-Apr-83
092	8	511-1701	SOCKET, IC 14 PIN U3	RP P 1	C P EA	750	28-Jul-81	14-Apr-83
093	8	511-2061	SOCKET, IC 20 PIN U4	RP P 1	C P EA	750	28-Jul-81	14-Apr-83
096	8	511-2061	SOCKET, PIN, SINGLE U5	RP P 1	C P EA	750	28-Jul-81	14-Apr-83

EFFICIENCY DATE: 4/1

PARENT PART: A9M1005

FG. PROFILE \*GENERIC\* DRIVE - EURO UM: EA PROD CODE: DH  
ECC: A SRC CODE: G TYPE: 1 ABC: \* FLAR CODE: F DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	PR S I S W P	UM	EXTIMDFP	QTY	DATE	START	DATE	QTY	DATE	QTY	DATE	QTY	DATE	QTY	DATE
087	8	515-0120	1A CONN,HDR,SSL ROW,4F	RP P 1	* P EA	0			C78128	Jul-81	0	02-Mar-82						
085	8	515-0130	1R CONN,HDR,RT ANG,DBL ROW,8/16F	RP P 1	* P EA	0			C78128	Jul-81	0							
088	8	515-0131	1F CONN,HDR,RT ANG,DBL ROW,17/34F	RP P 1	C P EA	0			C78101	Mar-82	0							
086	8	515-0140	1A CONN,HDR,RT ANG,5F,W/LKG RAMP	RP P 1	* P EA	0			C78128	Jul-81	0							
105	8	515-0380	1A CONN,HDR,RT ANG,DBL ROW,17/34F	**	** EA	0			C78129	Aug-83	0							
104	8	550-0101	1C TUBING, HEAT SHRINK 1/4 ID BLACK USE W/ALT P/N	EX X 7	P C P FT	0			C50308	Jul-83	0							
095	8	820-0054	AE PCB, ANALOG PROFILE	RP P 1	* P EA	0			F21401	Mar-82	0							
001	6	699-0054	A ASSY, O.E.M. HEAD DISC (H.D.A.)	VX A 1	P A P EA	0			600	14-Dec-82	0							
006	4	810-0090	1A DRESS PANEL, DRIVE, PROFILE	RM P 1	* P EA	0			F56714	Dec-82	0							
007	4	810-0091	1B DRESS PANEL, PWR SPLY PROFILE	RM P 1	* P EA	0			F64414	Dec-82	0							
012	4	825-0207	B LABEL, FCC NON COMPLIANCE APPLE 3	EX X 7	P C P EA	0			F59321	Mar-83	0							
004	3	656-6121	3B INACT,ASSY,CHASSIS,PROFILE-CLASS	**	** EA	1			L30512	Dec-83	1							
003	4	400-1606	1C SCR 6-32X3/8 PN HD CRS REC STL ZN	EX X 1	P C P EA	1			C54012	Dec-83	1							
013	4	403-1606	1C SCR 6-32X3/8 PN HD CRS REC STL BL ZI	EX X 7	S C U EA	16			C54012	Dec-83	1							
009	4	430-1001	1C SCR TAP 8-18X.437 PN CRS STL ZN	EX X 7	P C P EA	3			C54012	Dec-83	3							
002	4	656-5121	3A INACT,SURASSY,BASE,PROFILE-CLASS	**	** EA	1			L30512	Dec-83	1							
005	5	400-1604	1C SCR 6-32X1/4 PN HD CRS REC STL ZN	EX X 7	C P EA	2			C54012	Dec-83	2							
011	5	400-1608	1C SCR 6-32X1/2 PN HD CRS REC STL ZN	EX X 7	C P EA	1			C54012	Dec-83	1							
012	5	436-1006	1C SCR TAP 4-24X.250 PN CRS REC STL	**	** EA	1			C54012	Dec-83	1							
001	5	699-5010	1A FURCH ASSY,COATD BTH CUR,PRFLE-B	**	** EA	1			P67612	Dec-83	1							
001	6	656-5021	6A SURASSY COVER,BOTTOM,PROFILE	**	** EA	1			P40812	Dec-83	1							
002	7	805-0086	1A SHIELD,CSA PROFILE	**	** EA	1			P40801	Apr-83	1							
001	7	815-5008	1C COVER, BOTTOM, PROFILE	RM P 1	* P EA	1			F40801	Apr-83	1							
008	5	805-0104	A SUPPORT, PROFILE	RP P 1	* P EA	1			P16812	Dec-83	1							
002	5	805-5022	1A SUBPANEL,REAR,PROFILE	**	** EA	1			F64412	Dec-83	1							
003	5	810-0095	1A COVER DRIVE,BOTTOM,PROFILE	**	** EA	1			P40812	Dec-83	1							
004	5	865-0005	MA FOOT, .52HT, SQ	EX X 7	P C P EA	6			545	12-Dec-83	6							
015	4	656-5130	3D INACT,MFG SURASSY,COVER,PROFILE	**	** EA	1			L30506	Jan-84	1							
004	5	590-0047	1B CABLE, ASSY, LED, PROFILE	RP P 1	* P EA	1			F46414	Dec-82	1							
008	6	517-0041	1A CONN,RCPT,INSUL, DISPL,.2P	RP P 1	* U EA	1			F10931	Aug-81	1							
003	6	550-0010	A TUBING, BRAINED, 1/8 DIA.	EX X 7	* U IN	24,5000			C50331	Aug-81	2							
007	6	550-0101	1C TUBING, HEAT SHRINK 1/4 ID BLACK	EX X 7	P C P FT	1			C50331	Aug-81	1							
006	6	550-0107	1C TUBING, HEAT SHRINK 1/16 ID BLACK	EX X 7	P C P FT	1			C50331	Aug-81	1							
004	6	561-2600	B WIRE, BLACK, 26 AWG, 7 X 34	EX X 7	P * P FT	25			C01831	Aug-81	25							
005	6	561-2622	R WIRE, 26 AWG STRAND, RED	EX X 7	* U FT	25			C01831	Aug-81	25							
001	6	710-0004	MA LED, RED APPLE III DISKABLE	RP X 1	P C P EA	1			442	31-Aug-81	1							
002	6	815-0190	0 GROMET, PANEL MTG. FOR RECT. LAMP	RM X 1	P C P EA	0			L05112	Dec-83	0							
001	5	699-5011	1B FURCH ASSY,COATD TOP,CVR,PRFLE-R	**	** EA	1			P40812	Dec-83	1							
001	6	815-5007	1C COVER, TOP, PROFILE	RM P 1	* P EA	1			442	27-Apr-84	1							
005	5	815-0196	0 GROMET, PANEL MTG. FOR RECT. LAMP	RM X 1	P C P EA	0			P40812	Dec-83	0							
005	5	815-5007	1C COVER, TOP, PROFILE	RM P 1	* P EA	0			P40812	Dec-83	0							
005	5	825-5111	1B LABEL, LOGO 16MM BY 16MM	EX X 7	P C P EA	1			F51414	Dec-82	1							
004	5	825-5117	1B LABEL, NAMEPLATE, PROFILE	EX P 7	* P EA	1			F51414	Dec-82	1							
004	5	825-5119	1B LABEL, TOP PROFILE	EX P 7	* P EA	1			F51414	Dec-82	1							

26-Apr-83  
11-Dec-83  
15-Feb-83  
15-Feb-83  
15-Feb-83



EFFECTIVITY DATE: ALL

J R D I W I T D B I L L S O F M A T E R I A L

PARENT PART: 49M1005

FG, PROFILE "GENERIC" DRIVE -- EURO UM: EA PROD CODE: DH ECH: P354 ASSEMBLY QTY: 1  
ERC: A SKUP CODE: N TYPE: J ARC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FRST S A P	EXTENDED	CHG	DATE	START	DATE	CLOSE
			REMARKS	CD C Y P B L U M	QTY PER					
003	5	830-0025	3A INACTIVE, REIDENTIFIED SEE 830-002	X * * P P EA	2	C61114		Dec-82		
002	5	835-0005	1R NUT, SPEED "J" TYPE SIZE 8	EX X 7 P C P EA	3	C74414		Dec-82		
001	4	656-5151	3A INACT. SUBASY, HDA/PWR SUP, PRFI-CLS	* * * * * EA	1	L30512		Dec-83		
004	5	159-0001	R TOROID, FERRITE	EX P 1 P C P EA	2	P-4		Dec-83		
003	5	341-0171	A MICROFCSR-2K FROG ROM FOUR PROFIL	* * * * * EA	1	P26612		Dec-83		
001	5	456-5111	3B INACT. SUBASY, PWR SPLY, PROFILE-CLS	* * * * * EA	1	L30512		Dec-83		
007	6	400-1603	1C SCR 6-32X3/16 FN HD CRS REC STL Z	EX P 7 * P EA	1	C54012		Dec-83		
008	6	400-1606	1C SCR 6-32X3/8 FN HD CRS REC STL ZN	EX X 1 P C P EA	1	C54012		Dec-83		
009	6	564-0010	1A STRAP, GROUND, BRAIDED, 2.75" LON	* * * * * EA	1	C70712		Dec-83		
006	6	656-4102	MC ASSY, PCB TSTD, CONTROLLER	WT A 1 * P EA	1	P26612		Dec-83		
002	7	337-8603	B IC SOCKET MICROPRO. W/24P FIGGYBA	RL P 1 * P EA	1	C14805		Mar-82		14-Oct-82
			U25							
001	7	656-0102	1M ASSY, PCB, UNSTD, CONTROLLER, PROFIL	WU A 1 * P EA	1	F65131		Aug-81		
000	8	050-5006	1E SCHEMATIC, CONTROLLER RD, PROFILE	D D 7 * U EA	0	F65104		Jan-82		
063	8	101-4101	1A RES 100 OHM 1/4W 5Z	RP P 1 P C P EA	2	C67531		Aug-81		
			R20, R21							
038	8	101-4102	1A RES 1K OHM 1/4W 5Z	RP P 1 P C P EA	1	C67531		Aug-81		14-Oct-83
			R15							
016	8	101-4103	1A RES 10K OHM 1/4W 5Z	RP P 1 P C P EA	1	C67531		Aug-81		
			R19							
036	8	101-4152	1A RES 1.5K OHM 1/4W 5Z	RP P 1 P C P EA	2	C67531		Aug-81		
			R9, R10							
040	8	101-4201	1A RES 200 OHM 1/4W 5Z	RP P 1 P C P EA	1	C67531		Aug-81		
			R17							
042	8	101-4303	1A RES 30K OHM 1/4W 5Z	RP P 1 P C P EA	4	C67525		Mar-83		
			R1, R2, R4, R5							
037	8	101-4332	1A RES 3.3K OHM 1/4W 5Z	RP P 1 P C P EA	8	C67531		Aug-81		
			R3, R6, R7, R8, R11, R12, R13, R18							
075	8	101-4333	1A RES 33K OHM 1/4W 5Z	RP P 5 P C P EA	4	C675				24-Mar-83
			R1, R2, R4, R5							
039	8	101-4392	1A RES 3.9K OHM 1/4W 5Z	RP P 1 P C P EA	1	C67531		Aug-81		14-Oct-83
			R1, R2, R4, R5							
041	8	101-4510	1A RES 51 OHM 1/4W 5Z	RP P 1 P C P EA	1	C67531		Aug-81		
			R14							
077	8	101-4512	1A RES 5.1K OHM 1/4W 5Z	RP P 1 P C P EA	1	C67531		Aug-81		
			R16							
035	8	111-0021	1A RES NETWORK 7 X 2K OHM 5Z	RP P 1 P C P EA	1	C67525		Mar-83		
			R22							
034	8	111-0022	1A RES NETWORK 7 X 10K OHM 5Z	RP P 1 P C P EA	1	C67531		Aug-81		
			RP1							
			RP2							
070	8	112-0102	1R RES ARRAY 8 X 47 OHM 10Z	RP P 1 P C P EA	2	C67531		Aug-81		12-Nov-81
001	8	112-0105	1R RES ARRAY 8 X 330 OHM	RP P 1 * P EA	2	C67513		Nov-81		06-Nov-83
			U1, U2							
001	8	112-0107	1R RES ARRAY 8 X 100 OHM	* * * * * EA	2	C67507		Nov-83		
			U1, U2							
041	8	121-0101	1P CAP ELECT 47UF 10% 100V	RP P 1 C P EA	4	C67531		Aug-81		
			U8, C21, C22, C30							
049	8	121-0102	1E CAP CER AXIAL 1UF 10% 25V	RP P 1 C P EA	31	C67531		Aug-81		
042	8	121-0103	1C CAP CER 100NF 10%	RP P 7 * P EA	1	C67531		Aug-81		14-Oct-81

ITEM LEVEL COMPONENT PART NUMBER

PARENT PART: 45M1005

FG, PROFILE 'GENERIC' DRIVE - EURO UM: EA  
ERC: A SRCE CODE: 6 TYPE: 1 ARC: \* PLAN CONF: F

ECN: P354 ASSEMBLY QTY: 1  
DATE: 15-Mar-83

ITEM DESCRIPTION EXTENDED QTY PER FROM START DATE TO CLOSE DATE

078 8 197-0502 1A CLOCK OSC, CRYSTAL 10 MHZ (TTL) \*\* \* \* EA 1 05-15-Oct-83  
080 8 197-0504 1A CLOCK OSCILLATOR, CRYSTAL, 10 MHZ \*\* \* \* EA 0 05-15-Oct-83  
ALT FOR ITEM 78

029 8 301-0006 A IC, 7406 EXP 7 \* P EA 1 06-31-Aug-81  
U41

009 8 305-0000 A IC, 74LS00N RIP 1 P B P EA 2 442 31-Aug-81  
U15, U26

026 8 305-0007 A IC, 74LS02N RIP 1 P B P EA 1 442 31-Aug-81  
U31

025 8 305-0008 A IC, 74LS08 RIP 1 P B P EA 1 442 31-Aug-81  
U32

017 8 305-0014 A IC, 74LS14 RIP 1 P B P EA 1 442 31-Aug-81  
U23

027 8 305-0038 A IC, 74LS38 QUAD 2 INPUT BUFFER RIP 1 P B P EA 1 649 31-Aug-81  
U24

019 8 305-0109 A IC, 74LS109 RIP 1 P B P EA 1 442 31-Aug-81  
U36

014 8 305-0153 A IC, 74LS153 RIP 1 P B P EA 1 442 31-Aug-81  
U6

006 8 305-0161 A IC, 74LS161 RIP 1 P B P EA 3 442 31-Aug-81  
U10, U16, U17

020 8 305-0163 A IC, 74LS163 RIP 1 P B P EA 1 442 31-Aug-81  
U22

013 8 305-0174 A IC, 74LS174 RIP 1 P B P EA 3 442 31-Aug-81  
U30, U34, U38

003 8 305-0240 A IC, 74LS240 RIP 1 B P EA 1 C12731-Aug-81  
U9

002 8 305-0244 A IC, 74LS244 RIP 1 P B P EA 2 442 31-Aug-81  
U4, U5

010 8 305-0257 A IC, 74LS257 RIP 1 P B P EA 2 442 31-Aug-81  
U13, U20

030 8 305-0280 A IC, 74LS280 9-BIT PARITY RIP 1 P B P EA 1 649 31-Aug-81  
U3

015 8 305-0323 A IC, 74LS323 RIP 1 P B P EA 1 442 31-Aug-81  
U14

047 8 305-0377 A IC, 74LS377 RIP 1 P B P EA 1 442 31-Aug-81  
U21

024 8 307-0074 A IC, 74S74 RIP 1 P B P EA 1 C06331-Aug-81  
U39

011 8 307-0086 A IC, 74S86 RIP 1 P B P EA 1 C06331-Aug-81  
U28

008 8 334-2114 IC IC 1024X4 STATIC RAM 2114 TST&ERN RIP 1 P C P EA 2 C62131-Aug-81  
U11, U18

000 8 062-0087 1E SPEC, 2114 RAM BURN-IN EX D 7 \* U FA 0 07-15-Jul-81

001 8 062-2114 1E 1024 X 4 STATIC RAM 2114 RL P 1 C P FA 2 07-15-Jul-81

002 8 062-0004 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

003 8 062-0005 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

004 8 062-0006 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

005 8 062-0007 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

006 8 062-0008 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

007 8 062-0009 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

008 8 062-0010 0 PART, 1024 X 4 (UNPROGRAMMED) RL P 1 P C P FA 1 07-15-Aug-81

12-Nov-81  
12-Nov-81  
12-Nov-81

EFFECTIVITY DATE: ALL

PARENT PART: 49M1005 FG, PROFILE 'GENERIC' DRIVE EURO UM: EA PROP CODE: DH ECN: P354 ASSEMBLY QTY: 1  
 ERC: A SRCO CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	QTY	UNIT	EXTENDED DT	PLAN CODE	ECN	DATE	CLOSE
004	8	337-8603	IC SOCKET MICROPRO. W/24P FIGGYBA RI P 1 * P EA	1				C14831-AUG-81	04-May-82	
018	8	337-9401	A CRC GENERATOR/CHECKER	1				642 31 AUG-81		
021	8	341-0066	A FROM, U29	1				P10513-NOV-81		
022	8	341-0067	A FROM, U37	1				P10513-NOV-81		
007	8	341-0068	A RAMPAL	1				P10513-NOV-81		
031	8	341-0080	U27 (OCT 16 INPT AND-OR-INVT GT ARY)	1						
074	8	341-0129	R PROG FROM 2K PROFILE CONTROLLER	1				P18413-NOV-81	04-May-82	
001	9	335-2716	A EPROM-FIRMWARE 3.90 Z8 PROFILE-27	1				P11031-AUG-81	12-Nov-81	
028	8	351-2074	A EPROM, 2048 X 8 2716	1				642 31-AUG-81		
023	8	359-4024	A QUAD DARLINGTON XSTR ARRAY 2074R	2				642 31-AUG-81		
033	8	371-4001	U7, U8 A VOLTAGE CONTROLLED MULTIVIBRATOR	1				642 31-AUG-81	14-Oct-83	
076	8	371-4128	U40 1A DIODE RECTIFIER IN4001 1.0A 50V	8				C59931-AUG-81		
064	8	371-4148	CR1-CR8 1A DIODE ZENER IN4128 250MW 60V	4				C53831-AUG-81	12-Nov-81	
062	8	400-1406	CR9-CR12 1C SCR 4-40X3/8 PN HD CRS REC STL ZN EX X 7 P C P EA	2				C54031-AUG-81		
055	8	511-1401	C SOCKET, IC 14 PIN	3				799 07-APR-83		
056	8	511-1601	C SOCKET, IC 16 PIN	11				799 31-AUG-81		
057	8	511-1801	C SOCKET, IC 18 PIN	2				799 31-AUG-81		
058	8	511-2001	C SOCKET, IC 20 PIN	7				799 31-AUG-81		
059	8	511-2401	C SOCKET, IC 24 PIN	1				799 31-AUG-81		
060	8	511-4001	C SOCKET, IC 40 PIN	1				799 31-AUG-81		
061	8	515-0005	1B CONN,PIN,SINGLE	9				C78131-AUG-81		
054	8	515-0053	1C CONN,HDR,STR,2P	1				C78131-AUG-81		
053	8	515-0082	P7 1A HEADER, 10 PIN RT ANGLE W/O EARS	1				C48031-AUG-81	16-Nov-82	
066	8	515-0150	P5 1A CONN,HDR,RT ANG,5P,.156 CTR,W/LKG	1				C78113-NOV-81		
067	8	515-0160	P3 1A CONN,HDR,RT ANG,2P,W/LKG RAMP	1				C78113-NOV-81		
065	8	515-0160	P4 1B CONN,FC TAIL,90 DEG,MET,LNG FTPRI	1				C78113-NOV-81		
049	8	520-0011	P1 1A CONN,FLUG,CONTACT KEY,D' SUB	1				C78131-AUG-81		
079	8	570-2339	P1 1A WIRE-STRANDED 22 AWG,GREEN,BULK	0.0420				C50915-OCT-83	14-Oct-83	
082	8	571-0001	P2 A WIRE BUS BAR, 70 AWG, .5 IN.	1				P0413-NOV-81		
047	8	571-0005	P3 1B PCB CONTROLER, PROFILE	1				P1431-AUG-81		
048	8	571-0100	P4 A WIP WASHB ASSY, STEPS 1-40	2				844 11-NOV-81		
041	8	571-0009	P5 1C PURCHASED ASSY,HOME SLIC PWR SUPPL	1				P7511-DEC-81		
042	8	571-0009	P6 A WIRE, WARDING PWR SUP PROFILE	1				P1112-DEC-81		
043	8	571-0009	P7 P. WARDING, PLY W/ 1/8 IN.	1				P1112-DEC-81		

DEFECTIVITY DATA: ALL  
 PARENT PART: 89M1005  
 FG. PROFILE \*GENERIC\* DRIVE - EURO UM: EA PROD CODE: 0H  
 SRC CODE: C TYPE: 1 ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FRS	TS	AF	UM	EXTENDED	CHG	NOTE	START	DATE	CLOSE	S/N
003	6	860-0213	1A STANDOFF, 6-32, 5/16", METAL JACKNUT	*	*	*	* EA	1						
002	5	656-5140	3B INACT. MFG. SUBASSY, H.D.A., PROFILE	*	*	*	* EA	1						
005	6	400-1604	1C SCF 6-32X1/4 FN HD CRS REC STL 7N	FX	X	7	C P EA	4						
004	6	590-0048	1R CABLE, ASSY, CNTRIF TO ANALOG PCB	RC	P	1	* P EA	1						
001	7	517-0070	1R CONN, CD ENG, IDC, 17/34P, W/O EAR	RP	P	1	* U EA	1						
002	7	517-0035	1R CONN, SRT, INSUL, 17/34P	RP	P	1	* U EA	1						
003	7	569-0204	1R CABLE, FLAT 34 CONDUCTOR	RC	P	1	* P FT	3,6200						
004	7	590-0053	3A IDENTIFY SEE 569-0204	RC	P	1	* P FT	3,6200						
002	6	590-0105	0 CABLE ASSY, #16 AWG GROUND WIRE	P	*	*	* P EA	1						
003	7	517-1102	1R TERMINAL, RING TORQUE #8	P	*	*	* P EA	1						
002	7	517-1211	1A TERMINAL, RECEFT 4.75 X .51 TAB	P	*	*	* P EA	1						
001	7	570-1601	A WIRE, 16 AWG, GRAY, 26/30, 4.80"	X	*	*	* P EA	1						
003	6	656-4101	A ASSY, PCB TSTD, ANALOG	WT	A	1	* P EA	1						
001	7	656-0101	1P ASSY, PCB UNSTGD, ANALOG, PROFILE	WU	A	1	* P EA	1						
000	8	050-5005	1J SCHEMATIC, ANALOG RD, PROFILE	D	D	7	* U EA	0						
050	8	101-4010	1A RES 1 OHM 1/4W 5Z	RP	P	1	S C P EA	1						
			R101											
051	8	101-4101	1A RES 100 OHM 1/4W 5Z	RP	P	1	F C P EA	2						
			R4,67											
053	8	101-4102	1A RES 1K OHM 1/4W 5Z	RP	P	1	F C P EA	19						
			R2-3, R15, R20-21											
			R38-39, R48, R54, R59											
			R60-62, R85-88											
			R106, R108											
058	8	101-4103	1A RES 10K OHM 1/4W 5Z	RP	P	1	P C P EA	11						
			R13, 17, 42-45, 47											
			R49, 70, 81, 117											
083	8	101-4104	1A RES 100K OHM 1/4W 5Z	RP	P	1	P C P EA	1						
			R115											
080	8	101-4111	1A RES 110 OHM 1/4W 5Z	RP	P	1	C P EA	2						
			R91, 92											
064	8	101-4121	1A RES 120 OHMS 1/4W 5Z	RP	P	1	P C P EA	2						
			R25, 26											
077	8	101-4122	1A RES 1.2K OHM 1/4W 5Z	RP	P	1	P C P EA	1						
			R107											
075	8	101-4123	1A RES 12K OHM 1/4W 5Z	RP	P	1	P C P EA	1						
			R73											
072	8	101-4151	1A RES 150 OHM 1/4W 5Z	RP	P	1	F C P EA	3						
			R36, 68, 114											
061	8	101-4152	1A RES 1.5K OHM 1/4W 5Z	RP	P	1	F C P EA	3						
			R7, 82, 83											
056	8	101-4182	1A RES 1.8K OHM 1/4W 5Z	RP	P	1	F C P EA	1						
			R69											
081	8	101-4201	1A RES 200 OHM 1/4W 5Z	RP	P	1	F C P EA	1						
			R110											
069	8	101-4202	1A RES 20.9K OHM 1/4W 5Z	RP	P	1	F C P EA	2						
			R12, 20											
067	8	101-4204	1A RES 22 OHM 1/4W 5Z	RP	P	1	F C P EA	3						
			R27, 31, 40											
065	8	101-4211	1A RES 240 OHM 1/4W 5Z	RP	P	1	F C P EA	2						

EFFECTIVITY DATE: 01  
 PARENT PART: APM1005  
 F9, PROFILE 'GENERIC' DRIVE - ELRO UM: EA PROD CODE: UM ECH: F354 ASSEMBLY QTY: 1  
 ERC: A SRCE CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM TYPE	COMPONENT PART NUMBER	PART DESCRIPTION	REMARKS	PRESTG AT	EXTENDED	QTY	UM	FCP	DATE	START	S/N	DATE	S/N
079	8	101-4242	1A RES 2.4K OHM 1/4W 5% R18,19	RP P 1 P C P EA	3		EA	C67528	Jul-81				
067	8	101-4242	1A RES 24K OHM 1/4W 5% R80,40,41	RP P 1 P C P EA	1		EA	C67528	Jul-81				
066	8	101-4244	1A RES 240K OHM 1/4W 5% R35	RP P 1 P C P EA	1		EA	C67528	Jul-81				
078	8	101-4272	1A RES 2.7K OHM 1/4W 5% R31	RP P 1 P C P EA	1		EA	C67528	Jul-81				
082	8	101-4301	1A RES 300 OHM 1/4W 5% R74	RP P 1 P C P EA	1		EA	C67528	Jul-81				
070	8	101-4331	1A RES 330 OHM 1/4W 5% R111	RP P 1 P C P EA	2		EA	C67528	Jul-81				
073	8	101-4332	1A RES 3.3K OHM 1/4W 5% R89,90	RP P 1 P C P EA	2		EA	C67528	Jul-81				
049	8	101-4390	1A RES 39 OHM 1/4W 5% R100,76	RP P 1 P C P EA	2		EA	C67528	Jul-81				
054	8	101-4391	1A RES 390 OHM 1/4W 5% R78,R112	RP P 1 P C P EA	1		EA	C67528	Jul-81				
060	8	101-4392	1A RES 3.9K OHM 1/4W 5% R55	RP P 1 P C P EA	7		EA	C67513	Apr-83				
052	8	101-4471	1A RES 470 OHM 1/4W 5% R9,8,113,1,27	RP P 1 P C P EA	4		EA	C67528	Jul-81				
084	8	101-4473	1A RES 47K OHM 1/4W 5% R118,119	RP P 1 P C P EA	2		EA	C67528	Jul-81				
065	8	101-4511	1A RES 510 OHM 1/4W 5% R37,52-53,77	RP P 1 P C P EA	5		EA	C67528	Jul-81				
071	8	101-4561	1A RES 560 OHM 1/4W 5% R116,71	RP P 1 P C P EA	1		EA	C67528	Jul-81				
045	8	101-4681	1A RES 680 OHMS 1/4W 5% R63,64,29,30,28	RP P 1 P C P EA	3		EA	C67528	Jul-81				
074	8	101-4751	1A RES 750 OHM 1/4W 5% R99	RP P 1 C P EA	2		EA	C67528	Jul-81				
063	8	101-4752	1A RES 7.5K OHM 1/4W 5% R11-12,R22	RP P 1 P C P EA	4		EA	C67528	Jul-81				
076	8	101-4822	1A RES 8.2K OHM 1/4W 5% R75,79	RP P 1 P C P EA	1		EA	C67528	Jul-81				
057	8	101-4823	1A RES 82K OHM 1/4W 5% R5,6,33,34	RP P 1 C P EA	1		EA	C67528	Jul-81				
048	8	108-1543	1A RES 1.54K OHM 1/4W 1% R72	RP P 1 P C P EA	1		EA	C75828	Jul-81				
042	8	108-1783	1A RES 1.78K OHM 1/4W 1% R46	RP P 1 C P EA	1		EA	C75828	Jul-81				
041	8	108-1863	1A RES 1.96K OHM 1/4W 1% R84	RP P 1 P C P EA	2		EA	C75901	Mar-82				
042	8	108-1863	1A RES 3.83K OHM 1/4W 1% R10	RP P 1 P C P EA	4		EA	C75901	Jul-81				
042	8	108-1863	1A RES 3.92K OHM 1/4W 1% R105,106	RP P 1 P C P EA	2		EA	C75901	Jul-81				
042	8	108-1863	1A RES 3.92K OHM 1/4W 1% R93,R94,95,97	RP P 1 P C P EA	2		EA	C75901	Jul-81				

IDENTIFIED MATERIAL

PARENT PART: ASH1005  
PART: PROFILE "GENERIC" DRIVE - EURO UM: EA PROP CODE: DH FUN: P354 ASSEMBLY QTY: 1  
SRC: A SRC CODE: 6 TYPE: 1 ARC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM	QUANTITY	COMPONENT	DESCRIPTION	FRST	START	CLOSE
LEVEL	PART NUMBER	REMARKS	UNIT	DATE	DATE	S/N
046	8	108-4531	1A RES 45.3 OHM 1/4W 1Z R14	RF P 1 C P EA	075828-Jul-81	
043	8	108-5623	1A RES 5.62K OHM 1/4W 1Z R24, R98	RF P 1 C P EA	075828-Jul-81	
106	8	109-0002	0 POT. 1F1M 1K OHM 20%	RF P 1 P C P EA	442 14-Oct-83	
040	8	109-0005	A POT. TRIM 500 OHM, 20% ALTN P/N 109-0420	RF P 1 * P EA	004518-Mar-82	09-Oct-83
098	8	109-0410	1A POT, 500 OHM 18 - 25 TURNS	RF P 1 C P EA	C50428-Jul-81	02-Mar-82
099	8	109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS ALTN P/N FOR ITEM 40	RF P 1 C P EA	F10518-Mar-82	09-Oct-83
038	8	111-0023	1A RES NETWORK 7 X 560 OHM 5% RF2-8	RF P 1 C P EA	067528-Jul-81	
094	8	111-0024	1A RES NETWORK 7 X 4.7K OHM 5% RF-1	RF P 1 C P EA	067528-Jul-81	
059	8	127-0100	1R CAP TANT 4.7 uF 20% 10V C59	RF P 1 * P EA	C59928-Jul-81	
037	8	127-0101	1R CAP TANT 10 uF 20% 15/16V C38-C40	RF P 1 * P EA	C59928-Jul-81	
029	8	130-0002	1R CAP CER AXIAL .01 UF +80%-20% 25V C12,67	RF P 1 P C P EA	C93928-Jul-81	
097	8	130-0003	1R CAP CER AXIAL .1 UF +80%-20% 25V C13,C14	RF P 1 P C P EA	C939	14-APR-83
028	8	130-0007	1R CAP CER AXIAL .1 UF +80%-20% 25V C3-5,10-16,21,22,25, C27,35-37,42-45,47 C48-51,53,55-57,63	RF P 1 C P EA	C93901-Mar-82	
031	8	130-0200	1A CAP CER .001 UF 10% 25V C24, C32	RF P 1 C P EA	C59928-Jul-81	
030	8	130-0201	1A CAP CER .0022 uF 10% 25V C19,23,28-31,26,62	RF P 1 C P EA	C59928-Jul-81	
036	8	137-5401	1A CAP DIP MICA 20 PF 5% 500V C61	RF P 1 C P EA	C54128-Jul-81	
035	8	137-5701	1A CAP DIP MICA 47 PF 5% 500V C34	RF P 1 P C P EA	C54128-Jul-81	
034	8	137-5801	1A CAP DIP MICA 75 PF 5% 500V CB	RF P 1 C P EA	C54128-Jul-81	
032	8	137-6101	1A CAP DIP MICA 100 PF 5% 500V C33	RF P 1 P C P EA	C54128-Jul-81	
033	8	137-6301	1A CAP DIP MICA 150 PF 5% 500V C9, C18, C17, C20	RF P 1 C P EA	C54128-Jul-81	
027	8	151-4701	1C INDUCTOR, 5.6 uH 10% L1, L2	RF P 1 * P EG	C39528-Jul-81	
021	8	156-0100	A DELAY LINE 14 PIN DIP 100 OHM, 50 DLY 2	RF P 1 * P EA	792 28-Jul-81	
022	8	156-0110	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1	RF P 1 * P EA	992 28-Jul-81	
002	8	156-0120	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1	RF P 1 * P EA	992 28-Jul-81	
003	8	156-0130	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1	RF P 1 * P EA	992 28-Jul-81	
004	8	156-0140	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1	RF P 1 * P EA	992 28-Jul-81	

EFFICIENCY RATE: ALL IDENTIFIERS OF MATERIAL

PARENT PART: A9M1005 FG, PROFILE "GENERIC" DRIVE - EURO UM: EA PROD CODE: DH FCM: F354 ASSEMBLY QTY: 1  
SRC: A SRC CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	COMPONENT PART NUMBER	DESCRIPTION	PRESTAP	EXTENDED	START	CLOSE
		REMARKS	QTY	QTY	DATE	DATE
005	8 305-0014	A IC, 74LS14 U30	RI P 1 P R P EA	1	442 28-Jul-81	
002	8 305-0174	A IC, 74LS174 U29	RI P 1 P R P EA	1	442 28-Jul-81	
004	8 307-0064	A IC, 74S64 U27	RI P 1 B P EA	1	C06328-Jul-81	
013	8 325-0102	A QUAD 2-INPUT NOR GATE U18	RI P 1 C P EA	1	741 28-Jul-81	
010	8 325-0107	A TRIPLE 2-INPUT EXCL OR/EXCL NOR GATE U10, U15	RI P 1 C P EA	2	741 28-Jul-81	
008	8 325-0114	A TRIPLE LINE RECEIVER U5, U14	RI P 1 C P EA	2	741 28-Jul-81	
009	8 325-0116	A TRIPLE LINE RECEIVER U26, U9	RI P 1 C P EA	2	741 28-Jul-81	
012	8 325-0117	A DL 2-WID 2-3-INPUT OR-AND/OR-AND-1 U16	RI P 1 C P EA	1	741 28-Jul-81	
011	8 325-0131	B IC ECL HIGH SPEED DUAL D FLIP-FLOP U11,17,19,20,21,22	RI P 1 C P EA	6	C25528-Jul-81	
006	8 327-0453	A IC, DUAL PERIPHERAL DRIVES U3	RI P 1 * P EA	1	757 28-Jul-81	
096	8 335-0007	A PROG HEX 16 INPT REG AND-OR GT AR U28	RL P 1 P B P EA	1	642 28-Jul-81	02-Mar-82
003	8 341-0069	A MEMFAL PROG HEX 16 INPT REG AND-OR GT AR U28	RL A 1 * P EA	1	P10501-Mar-82	
014	8 351-2907	A IC TRANS ARRAY QUAD PNP GEN PURPOSE U31, U23, U12	RP P 1 C P EA	3	750 28-Jul-81	
016	8 351-3127	A TRANSISTOR ARRAY NPN HIGH FREQ. U7	RP P 1 C P EA	1	750 28-Jul-81	
023	8 351-6700	A IC, TRANS. ARRAY QUAD COMP. PAIRS U1, U24	RI P 1 C P EA	2	750 28-Jul-81	
058	8 353-0005	A IC REG. +5V 100MA TO 92, 3 TERMINL RG1	RI P 1 C P EA	1	792 28-Jul-81	
018	8 353-0319	A IC, HIGH SPEED DUAL COMPARATOR U13	RI P 1 C P EA	1	750 28-Jul-81	
017	8 353-0353	A DUAL FET OF AMP/BUFFER U25, U8	RP P 1 C P EA	2	750 28-Jul-81	
015	8 353-0592	A IC, VIDEO AMPLIFIER U6	RI P 1 C P EA	1	750 28-Jul-81	
024	8 371-4152	1A DIODE FAST SWITCH 1N4152 500mW CR1-14, CR16-21, CR23-24, CR26	RP P 1 C P EA	23	C53828-Jul-81	
100	8 372-2222	1A TRANS,NPN, SWITCHING AND AMP ALT P/N FOR ITEM 23	* * * * EA	0	C40308-Jul-83	
101	8 372-2222	1A TRANS,NPN, SWITCHING AND AMP ALT P/N FOR ITEM 23	* * * * EA	0	C40308-Jul-83	
102	8 372-2222	1A TRANS,NPN, SWITCHING AND AMP ALT P/N FOR ITEM 23	* * * * EA	0	C40308-Jul-83	

EFFECTIVITY DATE: 011 IDENTIFIER: PILLIS OF MATERIAL A

PARENT PART: A9H1005

FG, PROFILE "GENERIC" DRIVE - EURO UM: EA PROD CODE: DH

ASSEMBLY QTY: 1

ERC: A SRCE CODE: G TYPE: 1

DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	FR ST S A P	EXTENDED	TOP DATE	START DATE	CLOSE DATE	S/N
103	8	372-3906	1B TRANSISTOR, PNP, SM, 8AMP, 2N3906	ALT P/N FOR ITEM 23 U24-QTY 2	RP P 1 P C P EA	0	C74908	JUL-83		
026	8	375-0010	1A DIODE REFERENCE 10mA 1.2V	ALT P/N FOR ITEM 23 U24-QTY 2	RP P 1 C P EA	1	C53828	JUL-81		
019	8	375-0012	1A DIODE DUAL VOLT VAR CAP 200mA 32V	CR15	RP P 1 * P EA	1	C53828	JUL-81		
020	8	376-0014	A FET, N-CHANNEL VOLT CONTRL RESIS.	Q2	RP P 1 * P EA	1	C30328	JUL-81		
090	8	511-0801	C SOCKET, IC 8 PIN	Q1	RP P 1 P C P EA	3	799 28	JUL-81	14-Apr-83	
091	8	511-1401	C SOCKET, IC 14 PIN		RP P 1 P C P EA	12	799 28	JUL-81	14-Apr-83	
092	8	511-1601	C SOCKET, IC 16 PIN		RP P 1 P C P EA	17	799 28	JUL-81	14-Apr-83	
093	8	511-2001	C SOCKET, IC 20 PIN		RP P 1 P C P EA	1	799 28	JUL-81	14-Apr-83	
089	8	515-0005	1R CONN, PIN, SINGLE		RP P 1 P C P EA	15	C78128	JUL-81		
087	8	515-0120	1A CONN, HDR, SGL ROW, 4P		RP P 1 * P EA	1	C78128	JUL-81	02-Mar-82	
085	8	515-0130	1R CONN, HDR, RT ANG, DBL ROW, 8/16P	J5	RP P 1 * P EA	1	C78128	JUL-81		
088	8	515-0131	1B CONN, HDR, RT ANG, DBL ROW, 17/34P	J5	RP P 1 C P EA	1	C78101	MAR-82	28-Aug-83	
086	8	515-0140	1A CONN, HDR, RT ANG, SP, W/LKG RAMP	J2	RP P 1 * P EA	3	C78128	JUL-81		
105	8	515-0380	1A CONN, HDR, RT ANG, DBL ROW, 17/34P	J6-B	* * * * EA	1	C78129	AUG-83		
104	8	550-0101	1C TUBING, HEAT SHRINK 1/4 ID BLACK	J2	EX X 7 P C P FT	0	C50308	JUL-83		
095	8	820-0054	AE PCB, ANALOG PROFILE	USE W/ALT P/N 100-101 ON U1	RP P 1 * P EA	1	F21401	MAR-82		
001	6	699-0054	A ASSY, O.E.M. HEAD DISC (H.D.A.)		VX A 1 P A P EA	1	600 14	DEC-82		
005	4	699-5011	1B PURCH ASSY, COATD TOP CUR, PROFILE-B		* * * * EA	1	L05112	DEC-83		05-Jan-84
001	5	815-5007	1C COVER, TOP, PROFILE		RM P 1 * P EA	1	F40812	DEC-83		
006	4	810-0090	1A DRESS PANEL, DRIVE, PROFILE		RM P 1 * P EA	1	F56712	DEC-83		
007	4	810-0091	1B DRESS PANEL, FWR SPLY PROFILE		RM P 1 * P EA	1	F64412	DEC-83		
012	4	825-0207	B LABEL, FCC NON COMPLIANCE APPLE 3		EX X 7 P C P EA	1	F59312	DEC-83		
014	4	835-0172	1A NUT, U TYPE .017 THK		* * * * EA	1	C67812	DEC-83		05-Jan-84
009	5	430-1012	1C SCR TAP 6-32X.312 FN CRS REC STL		X * * * EA	4	C54023	MAY-83		
021	3	825-0113	1B LABEL, CAUTION PROFILE/DIODE		EX P 7 * P EA	1	F46115	MAR-83		
011	3	825-0121	1B LABEL, PROFILE MODEL & SERIAL EUR		EX P 7 * P EA	1	F64815	MAR-83		
008	3	825-0122	C LABEL, INTDV, CARTON PROFILE EURO		EX X 7 P C P EA	1	F28415	MAR-83		
026	3	825-0311	1B LABEL, LOGO 16MM BY 16MM		EX X 7 P C P EA	1	F51415	MAR-83		
027	3	825-0313	1B LABEL, NAMEPLATE, PROFILE		EX P 7 * P EA	1	F51415	MAR-83		
028	3	825-0315	1C LABEL, LED PROFILE		EX P 7 * P EA	1	F51415	MAR-83		
010	3	825-0317	A LABEL, FRAGILE, PROFILE		EX P 7 * P EA	4	F11201	JUN-83		
020	2	825-0325	A LABEL, 210 VAC, 0.5 AMP		EX P 7 * P EA	1	F12015	MAR-83		
013	2	825-0328	A LABEL, DO NOT REMOVE END CAPS		EX P 7 * P EA	2	F12015	MAR-83		
015	2	825-0329	A LABEL, SERIAL NUMBER		EX P 7 * P EA	0.0000	F12015	MAR-83		
017	2	825-0050	B LABEL, BOARD, PALETTIZING, 2X2X16		EX X 7 S C U EA	0.3270	M58415	MAR-84		
018	2	825-0051	B LABEL, STRAPPING, 50 IN		EX X 7 S C P EA	0.1270	M58415	MAR-84		
019	2	825-0052	B LABEL, STRAPPING, CONTRAX 816		EX X 7 S A P EA	0.0000	M58415	MAR-84		



EFFECTIVITY DTD: ALL

INDEXED BILLS OF MATERIAL

PARENT PART: 49M1005

FG, PROFILE 'GENERIC' DRIVE - EURO  
ERC: A SRCO CODE: G TYPE: I

FCN: F354 ASSEMBLY QTY: 1  
DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FR S T S A F	UM	EXTENDED QTY PER	ECN	DATE	CLOSE	S/N
010	3	918-0071	B FALLET, 48 X 40 2 WAY ENTRY	EX P 7	B P EA	0.1670	M72515-Mar-83			
016	3	919-0012	A LABEL, MODEL TYPE 'EURO STD' RUBBER STAMP OR PEN	** ** *	** EA	1.3300	F33015-Mar-83			
012	3	942-0117	1C BOX, 29.5 X 21.25 X 16.13, PROFIL	EX X 7	C P EA	1	F39915-Mar-83		06-Jul-83	
022	3	942-0142	A BOX, OFF 19.25 X 10.75 X 6.88	EX P 7	* P EA	1	F12515-Mar-83		06-Jul-83	
025	3	944-0091	1A CUSHION BLOCK, EPS, PROFILE (TO REPLACE ACC KIT)	** ** *	** EA	1	F35415-Mar-83		06-Jul-83	
009	3	946-0003	R TAPE, P.S. 2 inch X 60 yard ALT FOR ITEM 24	EX X 7	P C P RL	0	C06415-Mar-83			
024	3	946-0010	A TAPE, SEALING GLASS WEB #341 ALT QTY .0150	EX X 7	R P RL	0.0100	883 15-Mar-83			
023	3	946-0011	A TAPE, PRESSURE SENSITIVE 2 INCH, AU ALT FOR ITEM 24	EX X 7	* P RL	0	C04915-Mar-83			
007	3	946-0012	1C STRAPPING, POLYPRO 1/2 INCH ALT QTY .0009	EX X 7	* P RI	0.0010	F72215-Mar-83			

EFFECTIVITY DATE: ALL INDEPEND BILLS OF MATERIAL

PARENT PART: AZM0305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: JH ECN: P354 ASSEMBLY QTY: 1  
ERC: B SRCO CODE: G TYPE: 1 ABC: \* PLAN CODE: F DATE: 15 Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	PART DESCRIPTION	FRST S A P	EXTENDED QTY PER	ECN	START DATE	CLOSE DATE	S/N
001 2	656-8101	D INACTIVE-FG, PROFILE FOR A3	DH G 1	A P EA	F33031	Aug-81	13-Dec-82	
017 3	600-0124	A INACTIVE, ASSY FOAM/CORR END PROF	EX P 7	* P EA	F12531	Aug-81	16-Oct-81	
018 3	600-0125	A INACTIVE, ASSY FOAM/CORR PROFILE	EX P 7	* P EA	F12531	Aug-81	16-Oct-81	
005 3	600-2513	A (INACTIVE) ASSY, BOTTOM PAD, PROF	WS A 1	* P EA	F26519	Oct-81	01-Dec-82	
006 3	600-2514	A (INACTIVE) ASSY, TOP PAD, PROFILE	WS A 1	* P EA	F26519	Oct-81	01-Dec-82	
004 3	600-2515	A ASSY, END PAD	WS A 1	* P EA	F12519	Oct-81	13-Dec-82	
014 3	600-2516	B ASSY, END CAP, PROFILE	WS A 1	* P EA	F56819	Oct-81	13-Dec-82	
021 3	600-2517	A ASSY, TOP/BOTTOM PAD, PROFILE	WS A 1	* P EA	F26502	Dec-82	13-Dec-82	
002 3	656-5103	C INACTIVE-SESY ACC FAC FG	WS A 1	* P EA	F33031	Aug-81	13-Dec-82	
009 4	030-0158	AB FORM, USFR INPT REPT FOR A3	EX X 7	P C P EA	A18631	Aug-81	13-Dec-82	
010 4	030-0183	1E REGIS. CARD, FERIPH. & SOFTWARE	EX X 7	P C P EA	A92731	Aug-81	13-Dec-82	
011 4	030-0272	1C MANUAL, USER'S, PROFILE FOR A3	EX P 7	C P EA	F63431	Aug-81	13-Dec-82	
007 4	030-0273	1D UNPACKING INSTRUCTIONS, PROFILE	EX X 7	C P EA	F72931	Aug-81	13-Dec-82	
008 4	030-0294	B PACKING LIST, PROFILE	EX X 7	* P EA	F31731	Aug-81	13-Dec-82	
018 4	031-0017	A NOTICE, PROFILE	EX P 7	* P EA	F13811	Feb-81	13-Dec-82	
020 4	031-0241	C PROFILE HELPFUL HINTS	EX X 7	* P EA	F17701	Mar-82	13-Dec-82	
004 4	590-0003	1B CABLE, A.C. POWER CORD	2H P 1	P C P EA	A86231	Aug-81	13-Dec-82	
003 4	590-0046	1B CABLE, ASSY, I/O PROFILE	RC P 1	* P EA	F60331	Aug-81	13-Dec-82	
001 5	519-0110	1A CONN, D*, IDC, 25P, W/O SR	RP P 1	* U EA	C78131	Aug-81	13-Dec-82	
002 5	569-0203	1B CABLE, FLAT 25 CONDUCTOR	RC P 1	* P FT	C52301	Oct-83	30-Sep-83	
003 5	590-0052	3A IDENTIFY SEE 569-0203	RC P 1	* P FT	C52331	Aug-81	13-Dec-82	
002 4	656-4103	A ASSY, PCB TSTD, I/O PROFILE A3	WT A 1	* P EA	F11331	Aug-81	13-Dec-82	
001 5	656-0103	1F ASSY, PCB UNSTD, I/O PROFILE, A3	WU A 1	* P EA	F78131	Aug-81	13-Dec-82	
000 6	050-5007	1B SCHEMATIC, I/O CARD, PROFILE	D D 7	* U EA	P65104	Jan-82	13-Dec-82	
015 6	101-4103	1A RES 10K OHM 1/4W 5%	RP P 1	P C P EA	C67531	Jul-81	13-Dec-82	
014 6	101-4332	1A RES 3.3K OHM 1/4W 5%	RP P 1	P C P EA	C67531	Jul-81	13-Dec-82	
029 6	101-4751	1A RES 750 OHM 1/4W 5%	RP P 1	C P EA	C67513	Nov-81	13-Dec-82	
034 6	112-0102	1B RES ARRAY 8 X 47 OHM 10%	RP P 1	P C P EA	C67531	Aug-81	12-Nov-81	
021 6	112-0104	1B RES ARRAY 7 X 470 OHM 5%	RP P 1	* P EA	C67531	Jul-81	12-Nov-81	
013 6	112-0105	1B RES ARRAY 8 X 330 OHM	RP P 1	* P EA	C67513	Nov-81	06-Nov-83	
036 6	112-0107	1B RES ARRAY 8 X 100 OHM.	* * *	* * EA	C67507	Nov-83	06-Nov-83	
035 6	130-0003	1B CAP CER AXIAL .1 UF +80%-20% 25V	RP P 1	P C P EA	C93913	Nov-81	17-May-82	
016 6	130-0007	1B CAP CER AXIAL .1 UF +80%-20% 25V	RP P 1	C P EA	C93918	May-82	17-May-82	
032 6	132-6101	1A CAP CER 100 PF 20% 50V	RP P 1	P C P EA	C54113	Nov-81	06-Nov-83	
031 6	159-0009	A HEAD, FERRITE	RP P 1	P C P EA	DC6213	Nov-81	06-Nov-83	
003 6	601-0000	1J	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
002 6	601-0001	1K	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
001 6	601-0002	1L	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0003	1M	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0004	1N	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0005	1O	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0006	1P	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0007	1Q	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0008	1R	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0009	1S	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0010	1T	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0011	1U	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0012	1V	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0013	1W	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0014	1X	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0015	1Y	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	
000 6	601-0016	1Z	RT P 1	P C P EA	C67531	Nov-81	13-Dec-82	

EFFECTIVITY DATE: 01

J N D E N T E D B I L L S O F M A T E R I A L

PARENT PART: A3M0305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: DH FCN: F354 ASSEMBLY QTY: 1  
ERC: B SRCE CONF: G TYPE: 1 ARC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	PRD QTY	SAFETY	EXTENDED QTY PER	FCN	DATE	START DATE	CLOSE DATE	S/N	
			C3										
			SUB F/N 301-0259										
			ITEM 28										
004	6	305-0010	A IC, 74LS10		RI	P	1	P	B	P	EA	1	442 31-Jul-81
002	6	305-0014	A IC, 74LS14		RI	P	1	P	B	P	EA	2	442 31-Jul-81
			A2, R4										
033	6	305-0038	A IC, 74LS38	QUAD 2 INPUT BUFFER	RI	P	1	P	B	P	EA	1	649 31-Aug-81
012	6	305-0109	A IC, 74LS109		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			R5										
005	6	305-0125	A IC, 74LS125		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			C4										
001	6	305-0132	A IC, 74LS132		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			A3										
006	6	305-0138	A IC, 74LS138		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			C2										
009	6	305-0244	A IC, 74LS244		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			A5										
010	6	305-0280	A IC, 74LS280	9-BIT PARITY	RI	P	1	P	B	P	EA	1	649 31-Jul-81
			A4										
011	6	305-0368	A IC, 74LS368		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			B6										
008	6	305-0374	A IC, 74LS374		RI	P	1	P	B	P	EA	1	442 31-Jul-81
			A6										
026	6	400-1406	1C SCR 4-40X3/8 PN HD CRS REC STL ZN		EX	X	7	P	C	P	EA	2	C54031-Jul-81
022	6	511-1401	C SOCKET, IC 14 PIN		RP	P	1	P	C	P	EA	8	799 31-Jul-81
023	6	511-1601	C SOCKET, IC 16 PIN		RP	P	1	P	C	P	EA	6	799 31-Jul-81
024	6	511-2001	C SOCKET, IC 20 PIN		RP	P	1	P	C	P	EA	2	799 31-Jul-81
025	6	515-0005	1B CORN, PIN, SINGLE	TP1, TP2	RP	P	1	P	C	P	EA	2	C78131-Jul-81
030	6	519-0100	1B CONN, PC TAIL, 90 DEG, MET, LNG	FTPRI	RP	P	1	*	P	EA	1	C78113-Nov-81	
			P1										
018	6	520-0011	1A CONN, PLUG, CONTACT KEY, 'D'	SUB	RP	P	1	C	P	EA	1	C78131-Jul-81	
			P1										
020	6	820-0056	AC PCB I/O, PROFILE, FOR A3		RM	P	1	*	P	EA	1	F13531-Jul-81	
027	6	835-0150	A NUT/WASHER ASSY, (NERS) 4-40		EX	P	7	*	P	EA	2	834 31-Jul-81	
005	4	681-0022	1E DISKETTE ASSY, A3 PROFILE DRIVER		WS	A	1	C	P	EA	1	L27302-Nov-81	
001	5	004-0039	1 DISKETTE, BLANK, WRITE PROTECTED		RD	P	1	P	C	P	EA	1	332 31-Aug-81
002	5	026-1010	1E LABEL, DISKWARE, A3 PROFILE DRIVE		EX	X	7	*	P	EA	1	L15131-Aug-81	
000	5	681-0001	C DISKETTE ASSY, SYSTEM UTILITIES		RO	A	1	P	C	P	EA	0	995 01-Mar-82
004	6	000-0000	1A NOT USED THIS ASSEMBLY		D	*	P	D	P	EA	0	NONE	
001	6	004-0039	1 DISKETTE, BLANK, WRITE PROTECTED		RD	P	1	P	C	P	EA	0	332 29-Jan-81
002	6	026-1002	C LABEL, DISKWARE SYSTEM UTILITIES		EX	X	7	P	C	P	EA	0	995 29-Jan-81
000	6	681-0001D	C DWG, DISKWARE ASSY APPLE 3		FX	D	7	*	U	EA	0	995	
003	6	014-0001	B ENVELOPE, DISKETTE APPLE 3		EX	X	7	P	C	P	EA	0	568 29-Jan-81
004	6	014-0001	B ENVELOPE, DISKETTE APPLE 3		EX	X	7	P	C	P	EA	1	568 29-Jan-81
005	6	014-0001	B ENVELOPE, DISKETTE APPLE 3		EX	X	7	P	C	P	EA	1	568 29-Jan-81
006	6	004-0002	1 DISKETTE, BLANK, A3 PROFILE 'DEMO'		WS	A	1	C	P	EA	1	C78131-Jul-81	
007	6	004-0002	1 DISKETTE, BLANK, WRITE PROTECTED		RD	P	1	P	C	P	EA	1	332 31-Aug-81
008	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
009	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
010	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
011	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
012	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
013	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
014	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	
015	6	004-0002	1E LABEL, DISKWARE, A3 PROFILE 'DEMO'		EX	X	7	*	P	EA	1	C78131-Jul-81	

13-Dec-82

13-Dec-82

J N D E N T E D B I L L S O F M A T E R I A L

PARENT PART: A3M0305 PRT: 3 PROFILE FOR APPLE /// ERM: H SRCE CONF: 6 TYPE: 1 UM: EA FROM CODE: 0H ECH: F354 ASSEMBLY QTY: 1 DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	QTY	UNIT	EXTENDED QTY PER	CHG	DATE	DATE	S/N
004	000-0000	1A NOT USED THIS ASSEMBLY	0	EA	0	NONF			
001	004-0034	1 DISKETTE, BLANK, WRITE PROTECTED	0	EA	0	332	29-Jan-81		
002	026-1002	C LABEL, DISKWARE SYSTEM UTILITIES	0	EA	0	995	29-Jan-81		
000	681-0001D	C TMG, DISKWARE ASSY APPLE 3	0	EA	0	995			
003	914-0019	B ENVELOPE, DISKETTE APPLE 3	0	EA	0	568	29-Jan-81		
003	914-0019	R ENVELOPE, DISKETTE APPLE 3	1	EA	1	568	19-Oct-81		
017	825-0324	MA LABEL, OPEN ME FIRST - PROFILE	1	EA	1	F12402	Nov-81		
016	825-0327	1B LABEL, ACC PAC PROFILE FOR A3	1	EA	1	F63902	Nov-81		13-Dec-82
019	825-0329	A LABEL, SERIAL NUMBER	1	EA	1	F12401	Mar-82		13-Dec-82
013	942-0047	R BAG, PLASTIC 8" X 12"	2	EA	2	C13731	Aug-81		13-Dec-82
001	942-0114	A BOX, ONE PIECE FOLDER	1	EA	1	F11331	Aug-81		13-Dec-82
012	942-0115	A BAG, BUBBLE 8 X 6	1	EA	1	F11331	Aug-81		13-Dec-82
014	946-0003	B TAPE, P.S. 2 inch X 60 yard	0.0120	RL	0.0120	C06431	Aug-81		13-Dec-82
015	946-0006	O TAPE, MASKING PERMACEL #P-786 3/4	0.0030	RL	0.0030	131	31-Aug-81		13-Dec-82
001	656-6101	AJ INACTIVE-CHASSIS ASY, A///	1	EA	1	F33031	Aug-81		13-Dec-82
033	341-0030	R PROG FROM 2K PROFILE CONTROLLER	1	EA	1	F18405	May-82		14-Oct-82
039	341-0171	A MICROPCSR-2K PROG ROM FORR PROFI	1	EA	1	F26615	Oct-82		13-Dec-82
022	400-1603	1C SCR 6-32X3/16 PN HD CRS REC STL Z	1	EA	1	C54001	Jul-82		13-Dec-82
021	400-1604	1C SCR 6-32X1/4 PN HD CRS REC STL ZN	10	EA	10	C54001	Jul-82		13-Dec-82
025	400-1606	1C SCR 6-32X3/8 PN HD CRS REC STL ZN	4	EA	4	C54001	Jul-82		13-Dec-82
024	400-1608	1C SCR 6-32X1/2 PN HD CRS REC STL ZN	5	EA	5	C54001	Jul-82		13-Dec-82
036	400-5603	B SCREW-BINDER HD PHILLIP 6-32 X 3/8	0	EA	0	C123			30-Jun-82
035	400-5604	B INACTIVE, SCREW, CRS RES BND 6-32X1	0	EA	0	C123			30-Jun-82
037	400-5608	B SCREW-BND HD PHL 6-32 X 1/2	0	EA	0	C123			30-Jun-82
038	403-5606	1C SCR 6-32X3/8 BND HD PHL RL ZINC	0	EA	0	C540			30-Jun-82
014	430-1001	1C SCR TAP 8-18X.437 FN CRS STL ZN	3	EA	3	C54031	Aug-81		13-Dec-82
026	430-1006	1C SCR TAP 4-20X.250 FN CRS REC STL	1	EA	1	C54031	Aug-81		13-Dec-82
011	590-0047	1B CABLE, ASSY, LED, PROFILE	1	EA	1	F46431	Aug-81		13-Dec-82
008	517-0041	1A CONN, RCPT, INSUL, DISPL, 2P	1	EA	1	C78131	Aug-81		13-Dec-82
003	550-0010	A TUBING, BRAIDED, 1/8 DIA.	24	EA	24	P10931	Aug-81		13-Dec-82
007	550-0101	1C TUBING, HEAT SHRINK 1/4 ID BLACK	2	EA	2	C50331	Aug-81		13-Dec-82
006	550-0103	1C TUBING, HEAT SHRINK 1/16 ID BLACK	1	EA	1	C50331	Aug-81		13-Dec-82
004	561-2600	B WIRE, BLACK 26 AWG, 7 X 34	25	EA	25	764	31-Aug-81		13-Dec-82
005	561-2622	B WIRE, 26 AWG STRAND, RED	25	EA	25	C01831	Aug-81		13-Dec-82
001	710-0004	MA LED, RED APPLE III DISK CABLE	1	EA	1	552	31-Aug-81		26-Apr-83
002	815-0190	O GROMET, PANEL MTG, FOR RECT. LAMP	0	EA	0	442	31-Aug-81		13-Dec-82
010	590-0048	1B CABLE, ASSY, CNTRLR TO ANALOG PCB	1	EA	1	P60331	Aug-81		13-Dec-82
001	513-0020	1B CONN, CD ENG, IDC, 17/34P, W/O EAR	1	EA	1	C78131	Aug-81		13-Dec-82
002	517-0038	1B CONN, SKT, INSUL, DISPL, 17/34P	1	EA	1	C78131	Aug-81		13-Dec-82
003	569-0204	1A CARLE, FLAT 34 CONDUCTOR	3.6200	EA	3.6200	C52301	Oct-83		13-Dec-82
004	590-0053	3A REIDENTIFY SEE 569-0204	1	EA	1	F26631	Aug-81		13-Dec-82
003	656-4102	MC ASSY, PCB TSTD, CONTROLLER	1	EA	1	C14805	May-82		14-Oct-82
002	337-8603	B IC SOCKET MICROPRO. W/24P PIGGYBA	1	EA	1				
001	500-0102	1B ASSY, PCB, INTSTP, CONTROLLER, PROFIL	1	EA	1	F68131	Aug-81		14-Oct-83
000	500-5000	1A SCH, MATE, CONTROLLER RD, PROFILE	0	EA	0	F65104	Jan-82		
000	500-5100	1A SCH, INT, ORB 1/4W 5Z	0	EA	0	F65104	Jan-82		
000	500-5100	1A SCH, INT, ORB 1/4W 5Z	0	EA	0	F65104	Jan-82		
000	500-5100	1A SCH, INT, ORB 1/4W 5Z	0	EA	0	F65104	Jan-82		

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	FRS	EXTENDED	CHG	DATE	S/N	CLOSE
			1 PART DESCRIPTION	REMARKS	RP P 1 P C P EA	QTY PER	DATE	DATE		
016	6	101-4103	1A RES 10K OHM 1/4W 5% R19		RP P 1 P C P EA	1	067531	AUG-81		
036	6	101-4152	1A RES 1.5K OHM 1/4W 5% R9,R10		RP P 1 P C P EA	2	067531	AUG-81		
040	6	101-4201	1A RES 200 OHM 1/4W 5% R17		RP P 1 P C P EA	1	067531	AUG-81		
042	6	101-4303	1A RES 30K OHM 1/4W 5% R1,R2,R4,R5		RP P 1 P C P EA	4	067525	MAR-83		
037	6	101-4337	1A RES 3.3K OHM 1/4W 5% R3,R6,R7,R8, R11,R12,R13,R18		RP P 1 P C P EA	8	067531	AUG-81		
075	6	101-4333	1A RES 33K OHM 1/4W 5% R1,R2,R4,R5		RP P 5 P C P EA	4	0675			24-MAR-83
039	6	101-4392	1A RES 3.9K OHM 1/4W 5% R14		RP P 1 P C P EA	1	067531	AUG-81		14-OCT-83
041	6	101-4510	1A RES 51 OHM 1/4W 5% R16		RP P 1 P C P EA	1	067531	AUG-81		
077	6	101-4512	1A RES 5.1K OHM 1/4W 5% R22		RP P 1 P C P EA	1	067525	MAR-83		
035	6	111-0021	1A RES NETWORK 7 X 2K OHM 5% RP1		RP P 1 P C P EA	1	067531	AUG-81		
034	6	111-0022	1A RES NETWORK 7 X 10K OHM 5% RP2		RP P 1 P C P EA	1	067531	AUG-81		
070	6	112-0102	1B RES ARRAY 8 X 47 OHM 10% U1,U2		RP P 1 P C P EA	2	067531	AUG-81		12-NOV-81
001	6	112-0105	1B RES ARRAY 8 X 330 OHM U1,U2		RP P 1 P C P EA	2	067513	NOV-81		06-NOV-83
081	6	112-0107	1R RES ARRAY 8 X 100 OHM U1,U2		* * * * *	2	067507	NOV-83		
043	6	125-5701	1R CAP ELECT 47 UF -10%+75% 10V C8,C21,C29,C30		RP P 1 C P EA	4	077231	AUG-81		
045	6	130-0007	1R CAP CER AXIAL .1 UF +80%-20% 25V A CRYSTAL, 10MHZ		RP P 1 C P EA	31	093907	APR-83		
032	6	197-0017	1A CRYSTAL, 10MHZ		EX P 7 * P EA	1	792 31	AUG-81		
078	6	197-0502	1A CLOCK OSC, CRYSTAL 10 MHZ (TTL)		* * * * *	1	057615	OCT-83		14-OCT-83
080	6	197-0504	1A CLOCK OSCILLATOR, CRYSTAL, 10 MHZ ALT FOR ITEM 78		* * * * *	0	058416	OCT-83		
029	6	301-0006	A IC, 7406 U41		EX P 7 * P EA	1	006331	AUG-81		
009	6	305-0000	A IC, 74LS00N U15,U26		RI P 1 P B P EA	2	442 31	AUG-81		
026	6	305-0002	A IC, 74LS02N U31		RI P 1 P B P EA	1	442 31	AUG-81		
025	6	305-0008	A IC, 74LS08 U32		RI P 1 P B P EA	1	442 31	AUG-81		
012	6	705-0010	A IC, 74LS14 U27		RI P 1 P B P EA	1	442 31	AUG-81		
010	6	745-0000	A IC, 74LS30 QUAD 2 INPUT BUFFERS U24		RI P 1 P B P EA	1	442 31	AUG-81		
010	6	745-0100	A IC, 74LS10 U25		RI P 1 P B P EA	1	442 31	AUG-81		



DEPENDENT BILLS OF MATERIAL

3 PROFILE FOR APPLE /// UM: EA PROD CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ERC: R SRCE CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	COMPONENT PART NUMBER	PART DESCRIPTION	FRSTSAP	EXTENDET	FOR	START	CLOSE
		REMARKS	CDCTYFBIUM	QTY PER	CHK	DATE	S/N
033	371-4001	1A DIODE RECTIFIER 1N4001 1.0A 50V	RP P 1 P C P EA	8	C59931	Aug-81	
076	371-4128	1A DIODE ZENER 1N4128 250mW 60V	RP P 1 * P EA	4	C53831	Aug-81	12-Nov-81
064	371-4148	A DIODE FAST SWITCH 1N4148 200ma 75	RP P 1 P C P EA	4	C5381X	Nov-81	
062	400-1406	1C SCR 4-40X3/8 PN HD CRS REC STL ZN	EX X 7 P C P EA	2	C54031	Aug-81	
055	511-1401	C SOCKET, IC 14 PIN	RP P 1 P C P EA	3	799 07	Apr-83	
056	511-1601	C SOCKET, IC 16 PIN	RP P 1 P C P EA	11	799 31	Aug-81	
057	511-1801	C SOCKET, IC 18 PIN	RP P 1 P C P EA	2	799 31	Aug-81	
058	511-2001	C SOCKET, IC 20 PIN	RP P 1 P C P EA	7	799 31	Aug-81	
059	511-2401	C SOCKET, IC 24 PIN	RP P 1 P C P EA	1	799 31	Aug-81	
060	511-4001	C SOCKET, IC 40 PIN	RP P 1 P C P EA	1	799 31	Aug-81	
061	515-0005	1B CONN,PIN,SINGLE	RP P 1 P C P EA	9	C78131	Aug-81	
054	515-0053	1C CONN,HDR,STR,2P	RP P 1 P C P EA	1	C78131	Aug-81	
053	515-0082	1A HEADER, 10 PIN RT ANGLE W/O EARS	RP P 1 C P EA	1	C48031	Aug-81	16-Nov-82
066	515-0150	1A CONN,HDR,RT ANG,5P,.156 CTR,W/LKG	RP P 1 * P EA	1	C78113	Nov-81	
067	515-0160	1A CONN,HDR,RT ANG,2P,W/LKG RAMP	RP P 1 * P EA	1	C78113	Nov-81	
065	519-0100	1B CONN,PC TAIL,90 DEG,MET,LNG FTFRI	RP P 1 * P EA	1	C78113	Nov-81	
049	520-0011	1A CONN,PLUG,CONTACT KEY,'D' SUB	RP P 1 C P EA	1	C78131	Aug-81	
079	570-2239	1A WIRE,STRANDED 22 AWG,GREEN,BULK	* * * FT	0.0420	C50915	Oct-83	
068	571-0001	A WIRE, RUS BAR, 20 AWG, .5 IN.	EX X 7 * U FT	1	P23213	Nov-81	14-Oct-83
046	820-0055	1D PCB, CONTROLLER, PROFILE	RP P 1 * P EA	1	P17631	Aug-81	
069	835-0150	A NUT/WASHER ASSY, (KEFS) 4-40	EX P 7 * P EA	2	834 13	Nov-81	
001	656-5101	AD INACTIVE-SRSY DRIVE W/ANA BD, TST	WS A 1 * P EA	1	P33031	Aug-81	13-Dec-82
005	400-1604	1C SCR 4-40X1/4 PN HD CRS REC STL ZN	EX X 7 C P EA	4	C54001	Jul-82	13-Dec-82
004	400-5404	C SCR 4-40X1/4 BINDER HD PHILLIPS	EX X 7 * P EA	2	C54031	Aug-81	30-Jun-82
008	400-5604	B INACTIVE,SCREW,CRS RES RND 6-32X1	EX X 7 P C P EA	0	C123		30-Jun-82
007	590-0100	A CABLE ASSY, #16 AWG GROUND WIRE	P * * P EA	1	F18001	Mar-82	13-Dec-82
003	517-1101	1R TERMINAL, RING TONGUE #8	P * * P EA	1	C34401	Mar-82	
002	517-1211	1A TERMINAL, RECEPT 4.75 X .51 TAB	P * * P EA	1	C62801	Mar-82	
001	570-1601	A WIRE, 16 AWG, GRAY, 26/30, 4.80'	X * * P EA	1	C05701	Mar-82	
002	656-4101	A ASSY, PCB TSTD, ANALOG	WT A 1 * P EA	1	F11131	Aug-81	13-Dec-82
001	656-0101	1F ASSY, PCB UNTESTD, ANALOG, PROFILE	WU A 1 * P EA	1	L05031	Aug-81	
000	050-5005	1J SCHEMATIC, ANALOG BD, PROFILE	D D 7 * U EA	0	F69701	Mar-82	
050	101-4010	1A RES 1 OHM 1/4W 5% R101	RP P 1 S C P EA	1	C67528	Jul-81	
051	101-4101	1A RES 100 OHM 1/4W 5% R4,67	RP P 1 P C P EA	2	C67528	Jul-81	
053	101-4102	1A RES 1K OHM 1/4W 5% R2,4,15,R20-21	RP P 1 P C P EA	19	C67528	Jul-81	
		PCB ASSY, R54,R59					
		PCB ASSY, R55-R81					
		PCB, R108					
		PCB ASSY, R48					

UNPLANNED BILLS OF MATERIAL

PARENT PART: A3M0305 3 PROFILE FOR APPLE /// UM: EA PROP CODE: OH ECH: F354 ASSEMBLY QTY: 1  
ERC: B SRCF CODE: G TYPE: 1 ABC: \* PLAN CODE: P DATE: 15-MAR-83

ITEM LEVEL	COMPONENT PART NUMBER	F PART DESCRIPTION	FR S T S A P CD C Y P B L UM	EXTENDED QTY PEP	ECP CHG	START DATE	S/N	CLOSE DATE	S/N
		R13,17,42-45,47 R49,70,81,117							
093	7 101-4104	1A RES 100K OHM 1/4W 5% R115	RP P 1 P C P EA	1	C67528	Jul-81			
080	7 101-4111	1A RES 110 OHM 1/4W 5% R91,92	RP P 1 C P EA	2	C67528	Jul-81			
064	7 101-4121	1A RES 120 OHMS 1/4W 5% R25,26	RP P 1 P C P EA	2	C67528	Jul-81			
077	7 101-4122	1A RES 1.2K OHM 1/4W 5% R107	RP P 1 P C P EA	1	C67528	Jul-81			
075	7 101-4123	1A RES 12K OHM 1/4W 5% R73	RP P 1 P C P EA	1	C67528	Jul-81			
072	7 101-4151	1A RES 150 OHM 1/4W 5% R36,68,114	RP P 1 P C P EA	3	C67528	Jul-81			
061	7 101-4152	1A RES 1.5K OHM 1/4W 5% R7,82,83	RP P 1 P C P EA	3	C67528	Jul-81			
056	7 101-4182	1A RES 1.8K OHM 1/4W 5% R69	RP P 1 P C P EA	1	C67528	Jul-81			
081	7 101-4201	1A RES 200 OHM 1/4W 5% R110	RP P 1 P C P EA	1	C67528	Jul-81			
069	7 101-4203	1A RES 20.0K OHM 1/4W 5% R16,50	RP P 1 P C P EA	2	C76028	Jul-81			
062	7 101-4220	1A RES 22 OHM 1/4W 5% R23,24,32	RP P 1 P C P EA	3	C67528	Jul-81			
055	7 101-4241	1A RES 240 OHM 1/4W 5% R18,19	RP P 1 P C P EA	2	C67528	Jul-81			
079	7 101-4242	1A RES 2.4K OHM 1/4W 5% R80,40,41	RP P 1 P C P EA	3	C67528	Jul-81			
067	7 101-4243	1A RES 24K OHM 1/4W 5% R35	RP P 1 P C P EA	1	C67528	Jul-81			
066	7 101-4244	1A RES 240K OHM 1/4W 5% R31	RP P 1 P C P EA	1	C67528	Jul-81			
078	7 101-4272	1A RES 2.7K OHM 1/4W 5% R74	RP P 1 P C P EA	1	C67528	Jul-81			
082	7 101-4301	1A RES 300 OHM 1/4W 5% R111	RP P 1 P C P EA	1	C67528	Jul-81			
070	7 101-4331	1A RES 330 OHM 1/4W 5% R89,90	RP P 1 P C P EA	2	C67528	Jul-81			
073	7 101-4332	1A RES 3.3K OHM 1/4W 5% R100,76	RP P 1 P C P EA	2	C67528	Jul-81			
049	7 101-4350	1A RES 39 OHM 1/4W 5% R78,R112	RP P 1 P C P EA	2	C67528	Jul-81			
054	7 101-4391	1A RES 390 OHM 1/4W 5% R55	RP P 1 P C P EA	1	C67528	Jul-81			
060	7 101-4392	1A RES 3.9K OHM 1/4W 5% R9,8,113,127	RP P 1 P C P EA	2	C67528	Jul-81			
063	7 101-4411	1A RES 470 OHM 1/4W 5% R116,117	RP P 1 P C P EA	4	C67528	Jul-81			
064	7 101-4412	1A RES 470 OHM 1/4W 5% R118,119	RP P 1 P C P EA	2	C67528	Jul-81			



EFFECTIVITY DATE: ALL IN DENIED BILLS OF MATERIAL

PART: 330305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: DH ECH: F354 ASSEMBLY QTY: 1  
ERC: B SRCE CODE: B TYPE: 1 ABC: \* FIAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	REMARKS	FR ST S A F CD C Y F B L U M	EXTENDED QTY PER	FCP CHC	START DATE	S/N	CLOSE DATE	S/N
065	7 101-4511	1A RES 510 OHM 1/4W 5% R116,71		RP P 1 P C P EA	5	C67528	Jul-81			
071	7 101-4561	1A RES 560 OHM 1/4W 5% R63,64,29,30,28 R99		RP P 1 P C P EA	1	C67528	Jul-81			
045	7 101-4681	1A RES 680 OHMS 1/4W 5% R11-12,R22		RP P 1 P C P EA	3	C67528	Jul-81			
074	7 101-4751	1A RES 750 OHM 1/4W 5% R75,79		RP P 1 P C P EA	2	C67528	Jul-81			
063	7 101-4752	1A RES 7.5K OHM 1/4W 5% R5,6,33,34		RP P 1 P C P EA	4	C67528	Jul-81			
076	7 101-4822	1A RES 8.2K OHM 1/4W 5% R72		RP P 1 P C P EA	1	C67528	Jul-81			
057	7 101-4823	1A RES 82K OHM 1/4W 5% R46		RP P 1 P C P EA	1	C67528	Jul-81			
048	7 108-1543	1A RES 1.54K OHM 1/4W 1% R84		RP P 1 P C P EA	1	C75828	Jul-81			
042	7 108-1783	1A RES 1.78K OHM 1/4W 1% R10		RP P 1 P C P EA	1	C75828	Jul-81			
041	7 108-1963	1A RES 1.96K OHM 1/4W 1% R105,104		RP P 1 * P EA	2	C75801	Mar-82			
047	7 108-3833	1A RES 3.83K OHM 1/4W 1% R93,R95-96,R97		RP P 1 * P EA	4	C75831	Jul-81			
039	7 108-3923	1A RES 3.92K OHM 1/4W 1% R65,66		RP P 1 P C P EA	2	C75828	Jul-81			
046	7 108-4531	1A RES 45.3 OHM 1/4W 1% R14		RP P 1 P C P EA	1	C75828	Jul-81			
043	7 108-5623	1A RES 5.62K OHM 1/4W 1% R94,R98		RP P 1 P C P EA	2	C75828	Jul-81			
106	7 109-0002	0 POT, TRIM 1K OHM 20%		RP P 1 P C P EA	1	442	10-Oct-83			
040	7 109-0005	A POT, TRIM 500 OHM, 20% ALTN P/N 109-0420		RP P 1 * P EA	1	C04518	May-82		09-Oct-83	
098	7 109-0410	1A POT, 500 OHM 18 - 25 TURNS		RP P 1 P C P EA	1	C50428	Jul-81		02-Mar-82	
099	7 109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS ALTN P/N FOR ITEM 40		RP P 1 P C P EA	0	F10518	May-82		09-Oct-83	
038	7 111-0023	1A RES NETWORK 7 X 560 OHM 5% RF2-8		RP P 1 P C P EA	7	C67528	Jul-81			
094	7 111-0024	1A RES NETWORK 7 X 4.7K OHM 5% RF-1		RP P 1 P C P EA	1	C67528	Jul-81			
059	7 127-0100	1B CAP TANT 4.7 uF 20% 10V C59		RP P 1 * P EA	1	C59928	Jul-81			
037	7 127-0101	1B CAP TANT 10 uF 20% 15/16V C38-C40		RP P 1 * P EA	3	C59928	Jul-81			
029	7 130-0002	1B CAP CER AXIAL .01 uF 480V-20% 25V C1,2,6,7		RP P 1 P C P EA	4	C93928	Jul-81			
067	7 140-0002	1B CAP CER AXIAL .1 uF 480V-20% 25V C13,C14		RP P 1 P C P EA	2	C939			14-Apr-82	
049	7 140-0006	1B CAP CER AXIAL .1 uF 480V-20% 25V C15,C16,C17,20,21,22,25		RP P 1 P C P EA	31	C93901	Mar-82			

PARENT PART: 43M0305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: MH FCN: F35A ASSEMBLY QTY: 1  
 ERC: B SRCE COMF: G TYPE: 1 ARC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	QTY PER	EXTENDED QTY PER	UNIT	FCN	DATE	S/N	CLOSE DATE
031	7 130-0200	1A CAP CER .001 uF 10% 25V C24, C32	2	2	RF P 1 C P EA	C59928	Jul-81		
030	7 130-0201	1A CAP CER .0022 uF 10% 25V C19,23,28-31,26,62	8	8	RF P 1 C P EA	C59928	Jul-81		
036	7 137-5401	1A CAP DIP MICA 20 pF 5% 500V C61	1	1	RF P 1 C P EA	C54128	Jul-81		
035	7 137-5701	1A CAP DIP MICA 47 pF 5% 500V C34	1	1	RF P 1 P C P EA	C54128	Jul-81		
034	7 137-5801	1A CAP DIP MICA 75 pF 5% 500V C8	1	1	RF P 1 C P EA	C54128	Jul-81		
032	7 137-6101	1A CAP DIP MICA 100 pF 5% 500V C33	1	1	RF P 1 P C P EA	C54128	Jul-81		
033	7 137-6301	1A CAP DIP MICA 150 pF 5% 500V C9, C18, C17, C20	4	4	RF P 1 C P EA	C54128	Jul-81		
027	7 151-4701	1C INDUCTOR, 5.6 uH 10% L1, L2	2	2	RF P 1 * P EA	C39528	Jul-81		
021	7 156-0100	A DELAY LINE 14 PIN DIP 100 OHM, 50 OHM, 50 DLY 2	1	1	* P EA	792 28	Jul-81		
022	7 156-0110	A DELAY LINE 14 PIN DIP 500 OHM 100 DLY 1	1	1	* P EA	792 28	Jul-81		
007	7 301-0045	A IC, 7445 U4	1	1	RI P 1 C P EA	C06328	Jul-81		
...	7 301-0074	A IC, 7474 U2	1	1	RI P 1 P C P EA	C06328	Jul-81		
005	7 305-0014	A IC, 74LS14 U30	1	1	RI P 1 P B P EA	442 28	Jul-81		
002	7 305-0174	A IC, 74LS174 U29	1	1	RI P 1 P B P EA	442 28	Jul-81		
004	7 307-0064	A IC, 74S64 U27	1	1	RI P 1 B P EA	C06328	Jul-81		
013	7 325-0102	A QUAD 2-INPUT NOR GATE U18	1	1	RI P 1 C P EA	741 28	Jul-81		
010	7 325-0107	A TRIPLE 2-INPUT EXCL OR/EXCL NOR GA U10, U15	2	2	RI P 1 C P EA	741 28	Jul-81		
008	7 325-0114	A TRIPLE LINE RECEIVER U5, U14	2	2	RI P 1 C P EA	741 28	Jul-81		
009	7 325-0116	A TRIPLE LINE RECEIVER U26, U9	2	2	RI P 1 C P EA	741 28	Jul-81		
012	7 325-0117	A DL 2-MID 2-3-INPUT OR-AND/OR-AND-I U16	1	1	RI P 1 C P EA	741 28	Jul-81		
011	7 325-0131	B IC ECL HIGH SPEED DUAL D FLIP-FLO U11,17,19,20,21,22	6	6	RI P 1 C P EA	C35528	Jul-81		
006	7 327-0453	A IC, DUAL PERIPHERAL DRIVES U3	1	1	RI P 1 * P EA	757 28	Jul-81		
004	7 335-0067	A 160G HEX 16 INPUT REG AND/OR GT U14	1	1	RI P 1 P B P EA	641 28	Jul-81		
003	7 341-0040	REG AND/OR-AND-I AKI U13	1	1	RI P 1 * P EA	641 28	Jul-81		

007 Mar-82

EFFECTIVITY DATE: 011 J N D E N T E D B I L L S O F M A T E R I A L

PARENT PART: A3M0305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ERC: R SRCE CODE: G TYPE: 1 ARC: # PLAN CODE: F DATE: 15-Mar-83

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	PR ST S A P	EXTENDED	ECN	START	DATE	CLOSE
			REMARKS	CD C Y P R L U M	QTY PER	CHG	DATE		
014	7	351-2907	4 IC TRANS ARRAY QUAD PNP GEN PURPOSE	RP P 1 C P EA	3	750	28-Jul-81		
			U31, U23, U12						
016	7	351-3127	A TRANSISTOR, ARRAY NPN HIGH FREQ.	RP P 1 C P EA	1	750	28-Jul-81		
			U7						
023	7	351-6700	A IC, TRANS. ARRAY QUAD COMP. PAIRS	RI P 1 C P EA	2	750	28-Jul-81		
			U1, U24						
058	7	353-0005	ITEM 100-103 ALT P/N	RI P 1 C P EA	1	792	28-Jul-81		
			RG1						
018	7	353-0319	A IC, HIGH SPEED DUAL COMPARATOR	RI P 1 C P EA	1	750	28-Jul-81		
			U13						
017	7	353-0353	A DUAL FET OP AMP/BUFFER	RP P 1 C P EA	2	750	28-Jul-81		
			U25, U8						
015	7	353-0592	A IC, VIDEO AMPLIFIER	RI P 1 C P EA	1	750	28-Jul-81		
			U6						
024	7	371-4152	1A DIODE FAST SWITCH 1N4152 500mW	30 RP P 1 C P EA	23	C53828	Jul-81		
			CR1-14, CR16-21, CR23-24, CR26						
100	7	372-2222	1A TRANS,NPN,SWITCHING AND AMP	2N222 ** ** EA	0	C40308	Jul-83		
			ALT P/N FOR ITEM 23						
101	7	372-2907	A XSTR,2N2907, PNP SWITCH & AMPLIFI	** ** EA	0	C25908	Jul-83		
			ALT P/N FOR ITEM 23						
102	7	372-3904	A TRANSISTOR,NPN SW.&AMP. 2N3904	RP P 1 P C P EA	0	C30308	Jul-83		
			ALT P/N FOR ITEM 23						
103	7	372-3906	1B TRANSISTOR,PNP SW.&AMP. 2N3906	RP P 1 P C P EA	0	C76808	Jul-83		
			U24-QTY 2						
			ALT P/N FOR ITEM 23						
026	7	375-0010	1A DIODE REFERENCE 10mA 1.2V	RP P 1 C P EA	1	C53828	Jul-81		
			CR15						
019	7	375-0012	1A DIODE DUAL VOLT VAR CAP 200mA 32V	RP P 1 * P EA	1	C53828	Jul-81		
			Q2						
020	7	376-0016	A FET, N-CHANNEL VOLT CONTRL RESIS.	RP P 1 * P EA	1	C30328	Jul-81		
			Q1						
090	7	511-0801	C SOCKET, IC 8 PIN	RP P 1 P C P EA	3	799	28-Jul-81		14-Apr-83
091	7	511-1401	C SOCKET, IC 14 PIN	RP P 1 P C P EA	12	799	28-Jul-81		14-Apr-83
092	7	511-1601	C SOCKET, IC 16 PIN	RP P 1 P C P EA	17	799	28-Jul-81		14-Apr-83
093	7	511-2001	C SOCKET, IC 20 PIN	RP P 1 P C P EA	1	799	28-Jul-81		14-Apr-83
089	7	515-0005	1E CONN,PIN,SINGLE	RP P 1 P C P EA	15	C78128	Jul-81		
087	7	515-0120	1A CONN,HDR,SGL ROW,4P	RP P 1 * P EA	1	C78128	Jul-81		02-Mar-82
085	7	515-0130	1B CONN,HDR,RT ANG,DBL ROW,8/16P	RP P 1 * P EA	1	C78128	Jul-81		
			JS						
098	7	515-0131	1E CONN,HDR,RT ANG,DBL ROW,17/34P	RP P 1 C P EA	1	C78101	Mar-82		28-Aug-83
			LV						
099	7	515-0140	1A CONN,HDR,RT ANG,SF,S/LE RAMP	RP P 1 * P EA	3	C78108	Jul-81		
			LV						
105	7	515-0149	1A CONN,HDR,RT ANG,DBL ROW,17/34P	* * * EA	1	C78109	Aug-83		

EFFECTIVITY DATE: ALL IDENTIFIED BILLS OF MATERIAL

PARENT PART: A3M0305

3 PROFILE FOR APPLE ///  
ERC: R SRC CODE: G TYPE: 1

UM: EA PROD CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ABC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	PER S T S A P	EXTENDED QTY PER	DATE	DATE	CLOSE
		REMARKS	C D C Y F B L U M		CHG	S/N	S/N
104	7	550-0101 TUBING, HEAT SHRINK 1/4 ID BLACK USE W/ALT P/N 100-101 ON U1	EX X 7 P C F T	0	C50308	Jul-83	
095	7	820-0054 AI PCB, ANALOG PROFILE	RP P 1 * P EA	1	F21401	Mar-82	
001	5	699-4054 A ASSY, TEST. OEM HEAD DISK (H.D.A.)	VX P 1 P A P EA	1	710 31	Aug-81	13-Dec-82
001	6	699-0054 A ASSY, O.E.M. HEAD DISC (H.D.A.)	VX A 1 P A P EA	1	600 15	May-81	
003	5	905-0089 AA BRACKET, SUPPORT, PROFILE	SP P 1 * P EA	1	P23431	Aug-81	30-Jun-82
006	5	XXX-XXX1 0 390 OHM RES ASSY, PCB, MTR CNTRL (PART OF ITEM 1)	* * D * EA	0	31	Aug-81	13-Dec-82
002	4	656-5102 B INACTIVE-SRSY, POWER SUPPLY	WS A 1 * P EA	1	F33031	Aug-81	13-Dec-82
009	5	400-3404 IC SCR 4-40X1/4 FLT HB CRS REC STL Z	EX P 7 * P EA	2	C54031	Aug-81	01-Mar-82
005	5	400-5604 B INACTIVE,SCREW,CRS RES BND 6-32X1	EX X 7 P C P EA	8	C12331	Aug-81	01-Mar-82
004	5	519-0034 IA CONN,RCPT,INTL,POWER	RP P 1 P C P EA	1	C78131	Aug-81	01-Mar-82
012	5	550-0101 IC TUBING, HEAT SHRINK 1/4 ID BLACK	EX X 7 P C P FT	0.3200	C50331	Aug-81	01-Mar-82
011	5	561-1806 R WIRE, 18 AWG, BLACK, 7 X 26	EX X 7 S C P FT	0.2400	764 31	Aug-81	01-Mar-82
017	5	561-2244 R WIRE, YELLOW, 22 AWG, 7 X 30	EX P 7 * P FT	0.1600	764 31	Aug-81	01-Mar-82
010	5	561-2255 R WIRE, GREEN, 22 AWG, 7 X 30	EX P 7 * P FT	0.1600	764 31	Aug-81	01-Mar-82
016	5	561-2277 R WIRE, VIOLET, 22 AWG, 7 X 30	EX P 7 * P FT	0.1600	764 31	Aug-81	01-Mar-82
018	5	561-2299 R WIRE, WHITE, 22 AWG, 7 X 30	EX P 7 * P FT	0.1600	764 31	Aug-81	01-Mar-82
002	5	590-0045 A CABLE ASSY, POWER SUPPLY, PROFILE	RC P 1 * P EA	1	P16931	Aug-81	01-Mar-82
007	6	515-0032 IA CONTACT,FIN,CRIMP SNAP-IN,.081 DI	RP P 1 C P EA	2	C78131	Aug-81	01-Mar-82
001	6	517-0060 IA CONN,RCPT,INSUL,DISPL.,SGL ROW,5P	RP P 1 D U EA	1	C78131	Aug-81	01-Mar-82
002	6	517-0061 IA CONN,RCPT,INSUL,DISPL.,SGL ROW,18	RP P 1 * U EA	1	C34431	Aug-81	01-Mar-82
004	6	517-1101 1R TERMINAL RING TONGUE #6	RP P 1 * P EA	1	C78131	Aug-81	01-Mar-82
003	6	520-0060 IA CONN,HOUSING,PIN,2P	RP P 1 * P EA	1	C78131	Aug-81	01-Mar-82
006	6	520-0080 IA CONN,COVER,IDC,5P,.156 CTR	RP P 1 * U EA	1	C78131	Aug-81	01-Mar-82
005	6	520-0091 IA CONN,COVER,IDC,18P,.156 CTR	RP P 1 * U EA	1	C78131	Aug-81	01-Mar-82
013	6	525-0015 IA CONN,PLUG,KEYING	RP P 1 * U EA	1	C78131	Aug-81	01-Mar-82
008	6	550-0010 A TUBING, BRAIDED, 1/8 DIA.	EX X 7 * U IN	5	F10931	Aug-81	01-Mar-82
010	6	550-0011 A TUBING, BRAIDED, 1/4 DIA.	EX X 7 * U IN	12.7500	F10931	Aug-81	01-Mar-82
011	6	550-0101 IC TUBING, HEAT SHRINK 1/4 ID BLACK	EX X 7 P C P FT	2	C50331	Aug-81	01-Mar-82
012	6	550-0104 IC TUBING, HEAT SHRINK 3/8 ID BLACK	EX X 7 P C P FT	4	C50331	Aug-81	01-Mar-82
014	6	561-1800 R WIRE, 18 AWG, BLACK, 7 X 26	EX X 7 S C P FT	2.3000	764 31	Aug-81	01-Mar-82
018	6	561-1822 R WIRE, 18 AWG, RED, 7 X 26	EX X 7 * U FT	0.5000	C01831	Aug-81	01-Mar-82
009	6	561-1855 R WIRE, 18 AWG, GREEN, 7 X 26	EX X 7 * U FT	1.1700	C01831	Aug-81	01-Mar-82
017	6	561-1866 R WIRE, 18 AWG, BLUE, 7 X 26	EX X 7 * U FT	1.1700	C01831	Aug-81	01-Mar-82
016	6	561-1877 R WIRE, 18 AWG, VIOLET, 7 X 26	EX X 7 * U FT	0.6300	C01831	Aug-81	01-Mar-82
015	6	561-1899 R WIRE, 18 AWG, WHITE, 7 X 26	EX X 7 * U FT	1.7000	C01831	Aug-81	01-Mar-82
013	5	656-4105 A ASSY, PCB TESTFD, MONITOR, PROFIL	A * * P EA	1	F10931	Aug-81	01-Mar-82
001	6	656-0106 A ASSY, FCR UNTESTD, MONITOR, PROFIL	WU A 1 * P EA	1	F10931	Aug-81	01-Mar-82
002	7	101-2473 1A RES 47K OHM 1/2W 5%	RP P 1 S C P EA	1	C67531	Aug-81	01-Mar-82
003	7	101-2560 1A RES 56 OHM 1/2W 5%	RP P 1 * P EA	1	C67531	Aug-81	01-Mar-82
005	7	101-4103 1A RES 10K OHM 1/4W 5%	RP P 1 P C P EA	1	C67531	Aug-81	01-Mar-82
008	7	101-4164 1A RES 100K OHM 1/4W 5%	RP P 1 P C P EA	3	C67531	Aug-81	01-Mar-82
006	7	101-4187 1A RES 1K OHM 1/4W 5%	RP P 1 P C P EA	1	C67531	Aug-81	01-Mar-82
004	7	101-4201 1A RES 2K OHM 1/4W 5%	RP P 1 P C P EA	1	C67531	Aug-81	01-Mar-82
007	7	101-4184 1A RES 10K OHM 1/4W 5%	RP P 5 P C P EA	1	C67531	Aug-81	01-Mar-82
010	7	101-4101 1A RES 10K OHM 1/4W 5%	RP P 1 * P EA	2	C59031	Aug-81	01-Mar-82
009	7	101-4102 1A RES 10K OHM 1/4W 5%	RP P 1 * P EA	1	C59031	Aug-81	01-Mar-82

EFFECTIVITY DATE: ALL

PARENT PART: AZM0305

3 PROFILE FOR APPLE ///

UM: EA

ECN: F354

ASSEMBLY QTY: 1

ERC: R SRC CODE: G TYPE: 1

DATE: 15-Mar-83

PLAN CODE: P

ITEM	LEVEL	COMPONENT PART NUMBER	DESCRIPTION	FRS	TSA	AP	EXTENDED	QTY	PPM	CHG	DATE	START	S/N	CLOSE	S/N
012	7	327-0011	A TRANSISTOR,NFN,OPTICALLY COUPLED	RI	P	1	* P EA	1		F10931	Aug-81			13-Dec-82	
013	7	353-8212	A VOLTAGE DETECTOR/INDICATOR 8 PIN	RI	P	1	* P EA	1		F10931	Aug-81			01-Mar-82	
015	7	371-4150	1A DIODE SWITCHING 1M4152 500MA 50V	RP	P	1	P C P EA	2		C71431	Aug-81			01-Mar-82	
014	7	371-5240	1B DIODE ZENER 1N5240B 500mW 10V	RP	P	1	* P EA	1		C72731	Aug-81			01-Mar-82	
011	7	372-3904	A TRANSISTOR,NFN SW.&AMP, 2N3904	RP	P	1	P C P EA	2		C30331	Aug-81			01-Mar-82	
001	7	820-0058	A PCB, MONITOR PROFILE	RP	P	1	* P EA	1		F10931	Aug-81			01-Mar-82	
001	5	699-0059	AF PURCH. ASSY, POWER SUPPLY PROFILE	UX	P	1	A P EA	1		F18131	Aug-81			01-Mar-82	
003	5	705-0010	B SWITCH, ROCKER SPST W/ON-OFF LEGE	RP	P	1	P C P EA	1		783 31	Aug-81			01-Mar-82	
007	5	805-0090	B HOUSING, FWR SPLY, PROFILE	RP	P	1	* P EA	1		F14331	Aug-81			01-Mar-82	
008	5	805-0091	B COVER, TOP, FWR SUPPLY, PROFILE	RP	P	1	* P EA	1		F16831	Aug-81			01-Mar-82	
014	5	805-0092	A BRACKET, MONITOR, PROFILE	RP	P	1	* P EA	2		F10631	Aug-81			01-Mar-82	
019	5	805-0096	A INSULATOR, POWER SUPPLY	RP	P	1	* P EA	1		F10931	Aug-81			01-Mar-82	
020	5	825-0320	A LABEL, WARNING FWR SUP PROFILE	EX	P	7	* P E	1		F10931	Aug-81			01-Mar-82	
006	5	835-0151	A NUT/WASHER ASSY, (KEPS) 6-32	EX	P	7	* P EA	2		834 31	Aug-81			01-Mar-82	
015	5	860-0210	MA STANDOFF, HEX 6-32 X 1/4	EX	P	7	* P EA	1		F10931	Aug-81			01-Mar-82	
006	4	805-0086	1C SURFANEL, REAR, PROFILE	RP	P	1	* P EA	1		F52631	Aug-81			13-Dec-82	
030	4	805-0104	A SUPPORT, PROFILE	RP	P	1	* P EA	1		F16801	Feb-82			13-Dec-82	
007	4	810-0090	1A DRESS PANEL, DRIVE, PROFILE	RM	P	1	* P EA	1		F56731	Aug-81			13-Dec-82	
008	4	810-0091	1B DRESS PANEL, FWR SPLY PROFILE	RM	P	1	* P EA	1		F64431	Aug-81			13-Dec-82	
009	4	810-0092	B COVER,DRIVE,BOTTOM,PROFILE	RM	P	1	* P EA	1		F16831	Aug-81			13-Dec-82	
004	4	815-5007	1C COVER, TOP, PROFILE	RM	P	1	* P EA	1		F40831	Aug-81			13-Dec-82	
005	4	815-5008	1C COVER, BOTTOM, PROFILE	RM	P	1	* P EA	1		F40831	Aug-81			13-Dec-82	
023	4	825-0113	1B LABEL,CAUTION PROFILE/DUOFILE	EX	P	7	* P EA	1		F46131	Aug-81			13-Dec-82	
019	4	825-0114	1E LABEL, PROFILE MODEL & SERIAL NO.	EX	P	7	* P EA	1		P63131	Aug-81			13-Dec-82	
027	4	825-0207	B LABEL, FCC NON COMPLIANCE APPLE 3	EX	X	7	P C P EA	1		P59331	Aug-81			13-Dec-82	
016	4	825-0311	1B LABEL, LOGO 16MM BY 16MM	EX	X	7	P C P EA	1		P51431	Aug-81			13-Dec-82	
017	4	825-0313	1E LABEL, NAMEPLATE, PROFILE	EX	P	7	* P EA	1		F51431	Aug-81			13-Dec-82	
018	4	825-0315	1C LABEL, LED PROFILE	EX	P	7	* P EA	1		F51431	Aug-81			13-Dec-82	
028	4	825-0316	AA INACT,LBL 120 VAC .8 AMP UL FWR S	EX	P	7	* P EA	1		F19731	Aug-81			09-May-82	
032	4	825-0320	A LABEL, WARNING FWR SUP PROFILE	EX	P	7	* P EA	1		F10901	Mar-82			13-Dec-82	
029	4	825-0329	A LABEL, SERIAL NUMBER	EX	P	7	* P EA	1		P12415	Nov-81			13-Dec-82	
034	4	830-0025	3A INACTIVE,REIDENTIFIED SEE 830-002	EX	X	7	* P EA	2		C61120	May-82			13-Dec-82	
013	4	835-0005	1B NUT, SPEED 'J' TYPE SIZE 8	EX	X	7	P C P EA	3		C74431	Aug-81			13-Dec-82	
020	4	860-0200	1C STANDOFF, PLASTIC .188"	EX	P	7	C P EA	5		C52031	Aug-81			13-Dec-82	
031	4	860-0210	MA STANDOFF, HEX 6-32 X 1/4	EX	P	7	* P EA	1		F10901	Mar-82			13-Dec-82	
015	4	865-0005	MA FOOT, .52HT, SQ	EX	X	7	P C P EA	6		545 31	Aug-81			13-Dec-82	
008	3	825-0116	C LABEL, INDIVIDUAL CARTON PROFILE	EX	P	7	* P EA	1		F28431	Aug-81			13-Dec-82	
011	3	825-0207	B LABEL, FCC NON COMPLIANCE APPLE 3	EX	X	7	P C P EA	1		F59331	Aug-81			13-Dec-82	
010	3	825-0317	A LABEL, FRAGILE, PROFILE	EX	P	7	* P EA	4		F11231	Aug-81			13-Dec-82	
015	3	825-0328	A LABEL, DO NOT REMOVE END CAPS	EX	P	7	* P EA	1		F12519	Oct-81			13-Dec-82	
016	3	825-0329	A LABEL, SERIAL NUMBER	EX	P	7	* P EA	0.2000		F12419	Oct-81			13-Dec-82	
020	3	942-0112	A INACTIVE, RAG, ANTI STAT 14 X 9	EX	X	7	C P EA	2		F12531	Aug-81			16-Oct-81	
003	3	942-0117	1C BOX, 29.5 X 21.25 X 16.13, PROFIL	EX	X	7	C P EA	1		F39931	Aug-81			13-Dec-82	
012	3	942-0142	A BOX, OFF 19.25 X 10.75 X 6.88	EX	P	7	* P EA	1		F12519	Oct-81			13-Dec-82	
019	3	944-0012	A INACTIVE,16MM PAD TOP,16X9X6	EX	X	7	* P EA	1		F12531	Aug-81			16-Oct-81	
013	3	944-0013	B LABEL, .52 inch x .60 yard	EX	X	7	* P EA	0.0126		C68419	Oct-81			13-Dec-82	
009	3	944-0014	A LABEL, SEALING GLASS WEB 1341 63	EX	X	7	P C P RL	0.6150		474 31	Aug-81			13-Dec-82	
002	2	944-0015	1C SEALING, POLYPROP 1/2 INCH	EX	X	7	* P RL	0.6004		F72219	Oct-81			13-Dec-82	
004	1	944-0016	1B LABEL,FRAGILE FOR APPLE ???	* * *	* * *	* * *	* * *	1		F35414	Dec-82			01-Sep-83	
004	1	944-0017	1C LABEL, TOP PAD	45	A	1	* P EA	2		F12514	Dec-82			01-Sep-83	

EFFECTIVITY DATE: 6/1 INDIKER BILLS OF MATERIAL

PARENT PART: A3M0305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: DH ECN: F354 ASSEMBLY QTY: 1  
ERC: K SROF CODE: G TYPE: 1 ARC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM	QUANTITY	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	FR	ST	TS	AP	BL	UM	EXTENDED QTY PER	ECN CHG	DATE	CLOSE DATE	S/N
012	3	600-2516	B ASSY, ERD CAP, PROFILE		MS	A	1	*	P	EA	2	F56814	Dec-82	01-Sep-83	
005	3	600-2517	A ASSY, TOP/BOTTOM PAD, PROFILE		*	*	*	*	EA		2	P26514	Dec-82	01-Sep-83	
001	3	656-6110	RE INACT. MFG. ASSY, CHASSIS, PROFILE		*	*	*	*	EA		1	L30514	Dec-82	01-Sep-83	
003	4	400-1604	1C SCR 6-32X1/4 FN HD CRS REC STL ZN EX X 7		C	P	EA				8	C54014	Dec-82	30-Aug-83	
008	4	400-1606	1C SCR 6-32X3/8 FN HD CRS REC STL ZN EX X 7		C	P	EA				8	C54001	Jun-83	30-Aug-83	
004	4	400-1608	1C SCR 6-32X1/2 FN HD CRS REC STL ZN EX X 7		C	P	EA				4	C54014	Dec-82	31-May-83	
013	4	403-1606	1C SCR 6-32X3/8 FN CRS REC STL BL ZI		EX	X	7	S	U	EA	16	C54031	Aug-83		
009	4	430-1001	1C SCR TAP 8-18X.437 FN CRS STL ZN		EX	X	7	P	C	EA	3	C54014	Dec-82		
011	4	599-0046	1B CABLE, ASSY, I/O PROFILE		RC	P	1	*	P	EA	1	F60314	Dec-82	14-Apr-83	
001	5	519-0110	1A CONN, D*, IDC, 25P, W/O SR		RP	P	1	*	U	EA	2	C78131	Aug-81		
002	5	569-0203	1B CABLE, FLAT 25 CONDUCTOR		*	*	*	*	FT		3,2500	C52301	Oct-83		
003	5	590-0052	3A REIDENTIFY SEE 569-0203		RC	P	1	*	P	FT	3,2500	C52331	Aug-81	30-Sep-83	
010	4	656-4103	A ASSY, PCB TSTD, I/O PROFILE A3		WT	A	1	*	P	EA	1	F11314	Dec-82	14-Apr-83	
001	5	656-0103	1F ASSY, PCB UNTSTD, I/O PROFILE, A3		MU	A	1	*	P	EA	1	F78131	Aug-81		
000	6	050-5007	1B SCHEMATIC, I/O CARD, PROFILE		D	I	7	*	U	EA	1	F65104	Jan-82		
015	6	101-4103	1A RES 10K OHM 1/4W 5% R4,5,7		RP	P	1	P	C	EA	3	C67531	Jul-81		
014	6	101-4332	1A RES 3.3K OHM 1/4W 5% R1,3,6		RP	P	1	P	C	EA	3	C67531	Jul-81		
029	6	101-4751	1A RES 750 OHM 1/4W 5% R2		RP	P	1	C	P	EA	1	C67513	Nov-81		
034	6	112-0102	1B RES ARRAY 8 X 47 OHM 10X		RP	P	1	P	C	EA	2	C67531	Aug-81	12-Nov-81	
021	6	112-0104	1B RES ARRAY 7 X 470 OHM 5% B1		RP	P	1	*	P	EA	1	C67531	Jul-81		
013	6	112-0105	1B RES ARRAY 8 X 330 OHM A7,B7		RP	P	1	*	P	EA	2	C67513	Nov-81	06-Nov-83	
036	6	112-0107	1B RES ARRAY 8 X 100 OHM A7,B7		*	*	*	*	EA		2	C67507	Nov-83		
035	6	130-0003	1B CAP CER AXIAL .1 UF +80%-20% 25V		RP	P	1	P	C	EA	17	C93913	Nov-81		
016	6	130-0007	1B CAP CER AXIAL .1 UF +80%-20% 25V C1-C17		RP	P	1	C	P	EA	17	C93918	May-82	17-May-82	
032	6	132-6101	1A CAP CER 100 PF 20% 50V C18		RP	P	1	P	C	EA	1	C54113	Nov-81		
031	6	159-0009	A BEAD, FERRITE L1		RP	P	1	P	C	EA	1	IC6213	Nov-81		
003	6	301-0038	A IC, 7438 B3		RI	P	1	P	C	EA	1	C06313	Nov-81		
028	6	301-0259	A IC, 74259 U13		RI	P	1	P	C	EA	0	C06331	Jul-81		
007	6	301-9334	A IC, 9334 C3		RI	P	1	P	C	EA	1	C06331	Jul-81		
004	6	305-0016	A IC, 74LS10 ITEM 28		RI	P	1	P	B	EA	1	441	31 Jul-81		
009	6	305-0014	A IC, 74LS14 A,4,6		RI	P	1	P	B	EA	2	441	31 Jul-81		
003	6	305-0013	A IC, 74LS59 INPUT BUFFER B,10		RI	P	1	P	B	EA	1	649	31 Aug-81		
001	6	305-0015	A IC, 74LS16 B,10		RI	P	1	P	B	EA	1	441	31 Jul-81		

EFFECTIVITY DATE: ALL

IDENTIFIED BILLS OF MATERIAL

PARENT PART: A3M0305  
 ECH: F354 ASSEMBLY QTY: 1  
 SRC CODE: G TYPE: 1  
 PLAN CODE: F DATE: 15-Mar-83

ITEM	COMPONENT	DESCRIPTION	PR ST S A P	EXTENDED	CHG	DATE	START	DATE	DATE	S/N	DATE	S/N				
LN	PART NUMBER	REMARKS	CD	CY	P	B	I	UM	QTY	PER	DATE	S/N				
005	6	305-0125	A	IC	74LS125	B5	RI	P	1	P	B	P	EA	1	442	31-Jul-81
						CA										
001	6	305-0132	A	IC	74LS172	A3	RI	P	1	P	B	P	EA	1	442	31-Jul-81
						C2										
006	6	305-0138	A	IC	74LS138	A5	RI	P	1	P	B	P	EA	1	442	31-Jul-81
						A4										
009	6	305-0244	A	IC	74LS244	B6	RI	P	1	P	B	P	EA	1	442	31-Jul-81
						A6										
010	6	305-0280	A	IC	74LS280	A4	RI	P	1	P	B	P	EA	1	649	31-Jul-81
						B6										
011	6	305-0368	A	IC	74LS368	A6	RI	P	1	P	B	P	EA	1	442	31-Jul-81
						A6										
008	6	305-0374	A	IC	74LS374	A6	RI	P	1	P	B	P	EA	1	442	31-Jul-81
						A6										
026	6	400-1406	IC	SCR	4-40X3/8 PN HD CRS REC STL ZN	EX X 7 P C P EA										
022	6	511-1401	C	SOCKET	IC 14 PIN	RP P 1 P C P EA										
023	6	511-1601	C	SOCKET	IC 16 PIN	RP P 1 P C P FA										
024	6	511-2001	C	SOCKET	IC 20 PIN	RP P 1 P C P EA										
025	6	515-0005	1B	CONN, PIN, SINGLE	TF1, TP2	RP P 1 P C P EA										
030	6	519-0100	1B	CONN, PC TAIL, 90 DEG, MET, LNG	FTPRI	RP P 1 * P EA										
018	6	520-0014	1A	CONN, PLUG, CONTACT KEY, D	SUB P1	RP P 1 C P EA										
020	6	820-0056	AC	PCB I/O, PROFILE, FOR A3		RM P 1 * P EA										
027	6	835-0150	A	NUT/WASHER ASSY, (KEPS) 4-40		EX P 7 * P EA										
002	4	650-5120	3D	INACT. MFG SUBASSY, BASE, PROFILE		* * * EA										
005	5	400-1604	1C	SCR 6-32X1/4 PN HD CRS REC STL ZN	EX X 7 C P EA											
006	5	400-1606	1C	SCR 6-32X3/8 PN HD CRS REC STL ZN	EX X 1 P C P EA											
011	5	400-1608	1C	SCR 6-32X1/2 PN HD CRS REC STL ZN	EX X 7 C P EA											
007	5	430-1006	1C	SCR TAP 4-20X.250 PN CRS REC STL	EX X 7 * P EA											
012	5	436-1006	1C	SCR TAP 4-24X.250 PN CRS REC STL	EX X 7 * * EA											
001	5	652-5021	6A	SUBASSY COVER, BOTTOM, PROFILE		* * * EA										
002	6	805-0086	1A	SHIELD, CSA PROFILE		* * * EA										
001	6	815-5008	1C	COVER, BOTTOM, PROFILE		RM P 1 * P EA										
002	5	805-0088	1C	SUBPANEL, REAR, PROFILE		RP P 1 * P EA										
008	5	805-0104	A	SUPPORT, PROFILE		RM P 1 * P EA										
010	5	810-0097	R	COVER, DRIVE, BOTTOM, PROFILE		RM P 1 * P EA										
003	5	810-0095	1A	COVER, DRIVE, BOTTOM, PROFILE		RM P 1 * P EA										
009	5	815-5008	1C	COVER, BOTTOM, PROFILE		RM P 1 * P EA										
004	5	865-0005	MA	FOOT, .52HT, SR		EX X 7 P C P EA										
005	4	865-5130	3D	INACT. MFG SUBASSY, COVER, PROFILE		* * * EA										
004	5	590-0047	1B	CABLE, ASSY, LED, PROFILE		RC P 1 * P EA										
003	6	512-0041	1A	CONN, PC TAIL, 90 DEG, MET, LNG	FTPRI	RP P 1 * P EA										
003	6	515-0001	1B	CONN, PIN, SINGLE	TF1, TP2	RP P 1 * P EA										
003	6	515-0001	1B	CONN, PIN, SINGLE	TF1, TP2	RP P 1 * P EA										
004	6	515-0001	1B	CONN, PIN, SINGLE	TF1, TP2	RP P 1 * P EA										
004	6	515-0001	1B	CONN, PIN, SINGLE	TF1, TP2	RP P 1 * P EA										
004	6	515-0001	1B	CONN, PIN, SINGLE	TF1, TP2	RP P 1 * P EA										

31-May-83  
22-Jun-83

31-Mar-83  
31-Mar-83

INDEXED BILLS OF MATERIAL

PARENT PART: A3M0305 3 PROFILE FOR APPLE /// UM: EA PROD CODE: DH ECN: P354 ASSEMBLY QTY: 1  
ERC: B SRC CODE: G TYPE: 1 ARC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	PART IDENTIFICATION	PPSTISAP	EXTENDED	ECN	START DATE	CLOSE DATE
		REMARKS	QUANTITY	QTY	CHG	DATE	DATE
001	6	710-0004	MA LFD, REF APPLE III DISCABLE	1	552	31-Aug-81	
002	6	815-0190	0 BROWNT, PANEL MTG. FOR RECT. LAMP	0	442	31-Aug-81	26-Apr-83
001	5	699-5011	1B PURCH ASSY-COATD TOP CUR,PRFLE-R	1	L05112	Dec-83	
001	6	815-5007	1C COVER, TOP, PROFILE	1	F40812	Dec-83	
008	5	815-0190	0 GROMET, PANEL MTG. FOR RECT. LAMP	1	442	27-Apr-83	
009	5	815-5007	1C COVER, TOP, PROFILE	0	P408		
005	5	825-0311	1R LABEL, LOGO 16MM BY 16MM	1	F51414	Dec-82	11-Dec-83
006	5	825-0313	1R LABEL, NAMEPLATE, PROFILE	1	F51414	Dec-82	15-Feb-83
007	5	825-0315	1C LABEL, LFD PROFILE	1	F51414	Dec-82	15-Feb-83
002	5	830-0025	3A INACTIVE, REIDENTIFIED SEE 830-002	2	C61114	Dec-82	
002	5	835-0005	1R NUT, SPEED .1" TYPE SIZE 8	3	C74414	Dec-82	
001	4	656-5150	3A INACT.MFG SUBASY,HBA/PWR SUP,PROF	1	L30514	Dec-82	
003	5	341-0171	A MICROPRCSR-2K PROG ROM FORR PROFIL	1	P26614	Dec-82	
001	5	656-5110	6C MFG SUBASSY, POWER SUPPLY, PROFIL	1	F55814	Dec-82	
007	6	400-1603	1C SCR 6-32X3/16 FN HD CRS REC STL Z	1	C54014	Dec-82	
006	6	656-4102	MC ASSY, PCB TSTD, CONTROLLER	1	P26614	Dec-82	
002	7	337-8603	R IC SOCKET MICROPRO. W/24P PIGGYBA	1	C14805	May-82	14-Oct-82
			U25				
001	7	656-0102	1M ASSY,FCR,UNTSTD,CONTROLLER,PROFIL	1	F65131	Aug-81	
000	8	050-5006	1E SCHEMATIC, CONTROLLER BD, PROFILE	0	F65104	Jan-82	
063	8	101-4101	1A RES 100 OHM 1/4W 5%	2	C67531	Aug-81	
			R20,R21				
038	8	101-4102	1A RES 1K OHM 1/4W 5%	1	C67531	Aug-81	14-Oct-83
			R15				
016	8	101-4103	1A RES 10K OHM 1/4W 5%	1	C67531	Aug-81	
			R19				
036	8	101-4152	1A RES 1.5K OHM 1/4W 5%	2	C67531	Aug-81	
			R9,R10				
040	8	101-4201	1A RES 200 OHM 1/4W 5%	1	C67531	Aug-81	
			R17				
042	8	101-4303	1A RES 30K OHM 1/4W 5%	4	C67525	Mar-83	
			R1,R2,R4,R5				
037	8	101-4332	1A RES 3.3K OHM 1/4W 5%	8	C67531	Aug-81	
			R3,R6,R7,R8,				
			R11,R12,R13,R18				
075	8	101-4333	1A RES 33K OHM 1/4W 5%	4	C675		24-Mar-83
039	8	101-4392	1A RES 3.9K OHM 1/4W 5%	1	C67531	Aug-81	14-Oct-83
			R1,R2,R4,R5				
			R14				
041	8	101-4510	1A RES 51 OHM 1/4W 5%	1	C67531	Aug-81	
			R16				
077	8	101-451	\$\$\$HLRQ\$HML)\$*				
			RS \$\$\$HH	1	C67525	Mar-83	
074	8	101-6021	1A RES 100 OHM 1/4W 5%	1	C67531	Aug-81	
			R1				
074	8	101-6022	1A RES 100 OHM 1/4W 5%	1	C67531	Aug-81	
			R2				
076	8	101-6015	1A RES 100 OHM 1/4W 5%	1	C67531	Aug-81	
			R3				



EFFECTIVITY DATE: ALL

INDENTED BILLS OF MATERIAL

PARENT PART: A3MG705      3      PROFILE FOR APPLE ///      UM: EA      PROD CODE: 0H      FCN: P354      ASSEMBLY QTY: 1  
 URC: 1      SERI CODE: 6      TYPE: 1      ABC: \*      PLAN CODE: P      DATE: 15-MAR-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR S T S A P	EXTENDED	ECH	START	CLOSE
		REMARKS	CH C Y P B L UM	QTY PER	CHG	DATE	DATE
081	8 112-0107	1B RES ARRAY 8 X 160 OHM U1,U2	* * * * EA	2	C67507	Nov-83	
043	8 125-5701	1B CAP ELECT 47 UF -10%+75% 10V C8,C21,C29,C30	RP P 1 C P EA	4	C77231	AUG-81	
045	8 130-0007	1B CAP CER AXIAL .1 UF +80%-20% 25V	RP P 1 C P EA	31	C93907	APR-83	
032	8 197-0017	A CRYSTAL, 10MHZ	EX P 7 * P EA	1	792 31	AUG-81	14-Oct-83
078	8 197-0502	1A CLOCK OSC,CRYSTAL 10 MHZ (TTL)	* * * * EA	1	C57315	OCT-83	
080	8 197-0504	1A CLOCK OSCILLATOR,CRYSTAL,10 MHZ ALT FOR ITEM 78	* * * * EA	0	C58416	OCT-83	
029	8 301-0006	A IC, 7406 U41	EX P 7 * P EA	1	C06331	AUG-81	
009	8 305-0000	A IC, 74LS00N U15,U26	RI P 1 P B P EA	2	442 31	AUG-81	
026	8 305-0002	A IC, 74LS02N U31	RI P 1 P B P EA	1	442 31	AUG-81	
025	8 305-0008	A IC, 74LS08 U32	RI P 1 P B P EA	1	442 31	AUG-81	
017	8 305-0014	A IC, 74LS14 U23	RI P 1 P B P EA	1	442 31	AUG-81	
027	8 305-0038	A IC, 74LS38 QUAD 2 INPUT BUFFER U24	RI P 1 P B P EA	1	649 31	AUG-81	
019	8 305-0109	A IC, 74LS109 U36	RI P 1 P B P EA	1	442 31	AUG-81	
014	8 305-0153	A IC, 74LS153 U6	RI P 1 P B P EA	1	442 31	AUG-81	
006	8 305-0161	A IC, 74LS161 U10,U16,U17	RI P 1 P B P EA	3	442 31	AUG-81	
020	8 305-0163	A IC, 74LS163 U22	RI P 1 P B P EA	1	442 31	AUG-81	
013	8 305-0174	A IC, 74LS174 U30,U34,U38	RI P 1 P B P EA	3	442 31	AUG-81	
003	8 305-0240	A IC, 74LS240 U9	RI P 1 B P EA	1	C12731	AUG-81	
002	8 305-0244	A IC, 74LS244 U4,U5	RI P 1 P B P EA	2	442 31	AUG-81	
010	8 305-0257	A IC, 74LS257 U13,U20	RI P 1 P B P EA	2	442 31	AUG-81	
030	8 305-0280	A IC, 74LS280 9-BIT PARITY U3	RI P 1 P B P EA	1	649 31	AUG-81	
015	8 305-0323	A IC, 74LS323 U14	RI P 1 P B P EA	1	442 31	AUG-81	
047	8 305-0377	A IC, 74LS377 U37	RI P 1 P B P EA	1	442 31	AUG-81	
024	8 305-0072	A IC, 74LS00 U39	RI P 1 P B P EA	1	C06331	NOV-81	
011	8 305-0096	A IC, 74LS00 U40	RI P 1 P B P EA	1	C06331	NOV-81	

INDETERMINED BILLS OF MATERIAL

EFFECTIVITY DATE: ALL PARENT PART: 6340305 3 PROFILE FOR APPELL 272 UM: EA PROD CODE: DH FCN: F354 ASSEMBLY QTY: 1  
ESC: W SPEC CODE: S TYPE: I ARC: \* PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	DESCRIPTION	PR ST S A P L UM	EXTENDED QTY PER	ECN CHG	START DATE	S/N	CLOSE DATE	S/N
000	9 062-0083	1E SPEC, C114 RAM BURN-IN	EX 0 7 * U EA	0	C31415	Jul-83			
001	9 333-2114	1F IC 1024 X 4 STATIC RAM 2114	RL P 1 C P EA	2	C43715	Jul-83			
073	8 335-0004	A PROM, 512 X 8 (UNPROGRAMMED)	RL P 1 P C P EA	1	C02131	Aug-81		12-Nov-81	
071	8 335-0006	A PROG OCT 16 INPT AND-OR-INVT GT A	RL P 1 P B P EA	1	642 31	Aug-81		12-Nov-81	
072	8 335-6309	A PROM, MMI 6309-1	RL P 1 P C P EA	1	C-6 31	Aug-81		12-Nov-81	
012	8 337-8253	MA PROGRAMMABLE INTERVAL TIMER U32	RL P 1 P A P EA	1	642 31	Aug-81			
004	8 337-8603	B IC SOCKET MICROPRO. W/24F PIGGYBA	RL P 1 * P EA	1	C14831	Aug-81		04-May-82	
018	8 337-9401	A CRC GENERATOR/CHECKER U25	RL P 1 P A P EA	1	642 31	Aug-81			
021	8 341-0066	A PROM, U29 U35	RL A 1 * P EA	1	P10513	Nov-81			
022	8 341-0067	A PROM, U27	RL A 1 * P EA	1	P10513	Nov-81			
007	8 341-0068	A RAMFAL	RL P 1 * P EA	1	P10513	Nov-81			
031	8 341-0080	B PROG FROM 2K PROFILE CONTROLLER	RL P 1 * P EA	1	P18413	Nov-81		04-May-82	
074	8 341-0129	A EFROM-FIRMWARE 3.90 Z8 PROFILE-27	RL A 1 * P EA	1	F11031	Aug-81		12-Nov-81	
001	9 335-2716	A EFROM, 2048 X 8 2716	RL P 1 P C P EA	1	642 31	Aug-81			
028	8 351-2074	A QUAD DARLINGTON XSTR ARRAY 2074B	RF P 1 P B P EA	2	642 31	Aug-81			
023	8 359-4024	A VOLTAGE CONTROLLED MULTIVIBRATOR	RI P 1 P B P EA	1	642 31	Aug-81		14-Oct-83	
033	8 371-4001	1A DIODE RECTIFIER 1N4001 1.0A 50V	RF P 1 P C P EA	8	C59931	Aug-81			
076	8 371-4128	1A DIODE ZENER 1N4128 250mW 60V	RF P 1 * P EA	4	C53831	Aug-81		12-Nov-81	
064	8 371-4148	A DIODE FAST SWITCH 1N4148 200ma 75	RF P 1 P C P EA	4	C53813	Nov-81			
062	8 400-1406	1C SCR 4-40X3/8 FN HD CRS REC STL	EX X 7 P C P EA	2	C54031	Aug-81			
055	8 511-1401	C SOCKET, IC 14 PIN	RF P 1 P C P EA	3	799 07	Apr-83			
056	8 511-1601	C SOCKET, IC 16 PIN	RF P 1 P C P EA	11	799 31	Aug-81			
057	8 511-1801	C SOCKET, IC 18 PIN	RF P 1 P C P EA	2	799 31	Aug-81			
058	8 511-2001	C SOCKET, IC 20 PIN	RF P 1 P C P EA	7	799 31	Aug-81			
059	8 511-2401	C SOCKET, IC 24 PIN	RF P 1 P C P EA	1	799 31	Aug-81			
060	8 511-4001	C SOCKET, IC 40 PIN	RF P 1 P C P EA	1	799 31	Aug-81			
061	8 515-0005	1R CONN, PIN, SINGLE	RF P 1 P C P EA	9	C78131	Aug-81			
054	8 515-0053	1C CONN, HDR, STR, 2F	RF P 1 P C P EA	1	C78131	Aug-81			
053	8 515-0082	1A HEADER, 10 PIN RT ANGLE W/O EARS	RF P 1 C P EA	1	C48031	Aug-81		16-Nov-82	
066	8 515-0150	1A CONN, HDR, RT ANG, 5P, .156 CTR, W/LKG	RF P 1 * P EA	1	C78113	Nov-81			
067	8 515-0160	1A CONN, HDR, RT ANG, 5P, .156 CTR, W/LKG	RF P 1 * P EA	1	C78113	Nov-81			
065	8 515-0190	1F CONN, FC 100, 20 PIN, METALING	RF P 1 * P EA	1	C78113	Nov-81			
068	8 515-0200	1A CONN, FC 100, 20 PIN, METALING	RF P 1 * P EA	1	C78131	Nov-81			

EFFECTIVITY DATE: ALL

PARENT PART: A3M0305  
PART DESCRIPTION: 0 TYPE: 1  
UM: EA FROM CODE: PH  
ABC: \* PLAN CODE: F

ITEM	LEVEL	COMPONENT PART NUMBER	F PART DESCRIPTION	REMARKS	PR S T S A P	CD C Y P B L U M	EXTENDED QTY PER	ECN CHG	DATE	START DATE	S/N	CLOSE DATE	S/N
068	8	571-0001	Ø WIRE, BUS BAR, 20 AWG, .5 IN.		EX X 7	* U FT	1	F23213	14-Dec-82	14-Dec-82		16-Aug-83	
046	8	820-0055	1Ø PCB, CONTROLLER, PROFILE		RF P 1	* P EA	1	F17631	14-Dec-82	14-Dec-82		16-Aug-83	
069	8	835-0150	A NUT/WASHER ASSY, (KEPS) 4-40		EX P 7	* P EA	2	834 13	14-Dec-82	14-Dec-82		16-Aug-83	
001	6	699-0059	AB FURCH. ASSY, POWER SUPPLY PROFILE		VX P 1	A P EA	1	F18114	14-Dec-82	14-Dec-82		16-Aug-83	
005	6	825-0320	A LABEL, WARNING FWR SUP PROFILE		EX P 7	* P EA	1	F10914	14-Dec-82	14-Dec-82		16-Aug-83	
002	6	860-0200	1Ø STANDOFF, PLASTIC .188"		EX P 7	C P EA	5	C52014	14-Dec-82	14-Dec-82		16-Aug-83	
011	6	860-0210	HA STANDOFF, HEX 6-32 X 1/4		EX P 7	* P EA	0	F109	14-Dec-82	14-Dec-82		16-Aug-83	
003	6	860-0213	1A STANDOFF, 5-32, 5/16", METAL JACKNUT		EX * *	* * EA	1	C32530	14-Dec-82	14-Dec-82		16-Aug-83	
008	6	918-0023	Ø 1/4" TAN DOT		EX X 7	S C U EA	0						
004	6	918-0025	ALTN P/N FOR ITEM 4		EX X 7	S C U BX	1						
009	6	918-0029	ALTN QTY 1		EX X 7	S C U EA	0						
010	6	918-0031	ALTN P/N FOR ITEM 4		EX X 7	S C U EA	0						
002	5	656-5140	Ø 1/4" WHITE DOT		EX X 7	S C U EA	0						
005	6	400-1604	ALTN QTY 1		EX X 7	S C U EA	0						
004	6	590-0048	3B INACT.MFG.SUBASSY,H.D.A.,PROFILE		* * *	* * EA	1	L30514	14-Dec-82	14-Dec-82		16-Aug-83	
001	7	513-0020	1C SCR 6-32X1/4 FN HD CRS REC STL ZN		EX X 7	C P EA	4	C54014	14-Dec-82	14-Dec-82		16-Aug-83	
002	7	517-0035	1B CABLE, ASSY, CNTRLR TO ANALOG PCB		RC P 1	* P EA	1	F60314	14-Dec-82	14-Dec-82		16-Aug-83	
003	7	569-0204	1R CONN, CD EDG, IDC, 17/34P, W/O EAR		RP P 1	* U EA	1	C78131	14-Dec-82	14-Dec-82		16-Aug-83	
004	7	590-0053	1R CONN, SKT, INSUL, DISPL. 17/34P		RP P 1	C U EA	1	C78131	14-Dec-82	14-Dec-82		16-Aug-83	
002	6	517-1102	1R CABLE, FLAT 3Ø CONDUCTOR		* * *	* * FT	3,6200	C52301	14-Dec-82	14-Dec-82		16-Aug-83	
002	7	517-1211	3A IDENTIFY SEE 569-0204		RC P 1	* P FT	3,6200	C523	14-Dec-82	14-Dec-82		16-Aug-83	
001	7	570-1601	A CABLE ASSY, #16 AWG GROUND WIRE		P * *	* P EA	1	P18014	14-Dec-82	14-Dec-82		16-Aug-83	
003	7	656-4101	1R TERMINAL, RING TONGUE #8		P * *	* P EA	1	C34401	14-Dec-82	14-Dec-82		16-Aug-83	
001	7	656-0101	1A TERMINAL, RECEPT 4.75 X .51 TAB		P * *	* P EA	1	C62801	14-Dec-82	14-Dec-82		16-Aug-83	
000	8	050-5005	A WIRE, 16 AWG, GRAY, 26/30, 4.80"		X * *	* P EA	1	C05701	14-Dec-82	14-Dec-82		16-Aug-83	
050	8	101-4010	A ASSY, PCB TSTD, ANALOG		WT A 1	* P EA	1	P11114	14-Dec-82	14-Dec-82		16-Aug-83	
051	8	101-4101	1P ASSY, PCB UNTSTD, ANALOG, PROFILE		MU A 1	* P EA	1	L05031	14-Dec-82	14-Dec-82		16-Aug-83	
053	8	101-4102	1J SCHEMATIC, ANALOG RD, PROFILE		D D 7	* U EA	0	P69701	14-Dec-82	14-Dec-82		16-Aug-83	
066	8	101-4103	1A RES 1ØHM 1/4W 5%		RP P 1	S C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
068	8	101-4104	R101		RP P 1	P C P EA	2	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
069	8	101-4105	1A RES 1ØOHM 1/4W 5%		RP P 1	P C P EA	19	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
070	8	101-4106	R4*67		RP P 1	P C P EA	11	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
071	8	101-4107	R2-3,R15,R20-21		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
072	8	101-4108	R38-39,R48,R54,R59		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
073	8	101-4109	R60-62,R85-88		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
074	8	101-4110	R105-2100		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
075	8	101-4111	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
076	8	101-4112	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
077	8	101-4113	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
078	8	101-4114	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
079	8	101-4115	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
080	8	101-4116	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
081	8	101-4117	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
082	8	101-4118	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	
083	8	101-4119	1ØOHM 1/4W 5%		RP P 1	P C P EA	1	C67528	14-Dec-82	14-Dec-82		16-Aug-83	

EFFECTIVITY DATE: ALL IDENTIFIED BILLS OF MATERIAL

PARENT PART: ASM0805 3 PROFILE FOR APPLE /// UM: FA PROD CODE: OH ECN: F354 ASSEMBLY QTY: 1  
ITEM B: REF CODE: 6 TYPE: 1 ARI: 1 PLAN CODE: P DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR S T S A P CD C Y P B L UM	EXTENDED QTY PFR	ECN CHG	START DATE	CLOSE DATE	S/N
064	8 101-4121	1A RES 120 OHMS 1/4W 5% R91,92	RP P 1 P C P EA	2	C67528	Jul-81		
077	8 101-4122	1A RES 1.2K OHM 1/4W 5% R25,26	RP P 1 P C P EA	1	C67528	Jul-81		
075	8 101-4123	1A RES 12K OHM 1/4W 5% R107	RP P 1 P C P EA	1	C67528	Jul-81		
072	8 101-4151	1A RES 150 OHM 1/4W 5% R73	RP P 1 P C P EA	3	C67528	Jul-81		
061	8 101-4152	1A RES 1.5K OHM 1/4W 5% R36,68,114	RP P 1 P C P EA	3	C67528	Jul-81		
056	8 101-4182	1A RES 1.8K OHM 1/4W 5% R7,82,83	RP P 1 P C P EA	1	C67528	Jul-81		
081	8 101-4201	1A RES 200 OHM 1/4W 5% R69	RP P 1 P C P EA	1	C67528	Jul-81		
069	8 101-4203	1A RES 20.0K OHM 1/4W 5% R110	RP P 1 P C P EA	2	C76028	Jul-81		
062	8 101-4220	1A RES 22 OHM 1/4W 5% R16,50	RP P 1 P C P EA	3	C67528	Jul-81		
055	8 101-4241	1A RES 240 OHM 1/4W 5% R23,24,32	RP P 1 P C P EA	2	C67528	Jul-81		
072	8 101-4242	1A RES 2.4K OHM 1/4W 5% R18,19	RP P 1 P C P EA	3	C67528	Jul-81		
067	8 101-4243	1A RES 24K OHM 1/4W 5% R80,40,41	RP P 1 P C P EA	1	C67528	Jul-81		
066	8 101-4244	1A RES 240K OHM 1/4W 5% R35	RP P 1 P C P EA	1	C67528	Jul-81		
078	8 101-4272	1A RES 2.7K OHM 1/4W 5% R31	RP P 1 P C P EA	1	C67528	Jul-81		
082	8 101-4301	1A RES 300 OHM 1/4W 5% R74	RP P 1 P C P EA	1	C67528	Jul-81		
070	8 101-4331	1A RES 330 OHM 1/4W 5% R111	RP P 1 P C P EA	2	C67528	Jul-81		
073	8 101-4332	1A RES 3.3K OHM 1/4W 5% R89,90	RP P 1 P C P EA	2	C67528	Jul-81		
049	8 101-4390	1A RES 39 OHM 1/4W 5% R100,76	RP P 1 P C P EA	2	C67528	Jul-81		
054	8 101-4391	1A RES 390 OHM 1/4W 5% R78,R112	RP P 1 P C P EA	1	C67528	Jul-81		
060	8 101-4392	1A RES 3.9K OHM 1/4W 5% R55	RP P 1 P C P EA	7	C67513	Apr-83		
052	8 101-4471	1A RES 470 OHM 1/4W 5% R9,8,113,1,27	RP P 1 P C P EA	4	C67528	Jul-81		
063	8 101-4511	1A RES 4.7K OHM 1/4W 5% R118,119	RP P 1 P C P EA	1	C67528	Jul-81		
065	8 101-4512	1A RES 47K OHM 1/4W 5% R37,57,58,59	RP P 1 P C P EA	1	C67528	Jul-81		
064	8 101-4513	1A RES 470K OHM 1/4W 5% R116,71	RP P 1 P C P EA	1	C67528	Jul-81		
065	8 101-4514	1A RES 4.7K OHM 1/4W 5% R117,118,119,120	RP P 1 P C P EA	1	C67528	Jul-81		

EFFECTIVITY DATE: ALL

DEPENDENT BILLS OF MATERIAL

PARENT PART: A3M0305

PROFIT FOR APPLE ??? UM: EA PROD CODE: DH ASSEMBLY QTY: 1  
FTR: SREF COM: S LDF: 1 APC: # PLAN CODE: P

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR S T S A P L UM	EXTENDD QTY PER	ECM CHG	START DATE	CLOSE DATE	S/N
045	8 101-4681	1A RES 880 OHMS 1/4W 5% R11-12,R27	RP P 1 P C P EA	3	C67528	Jul-81		
074	8 101-4751	1A RES 250 OHM 1/4W 5% R75,79	RP P 1 C P EA	2	C67528	Jul-81		
063	8 101-4752	1A RES 7.5K OHM 1/4W 5% R5,6,33,34	RP P 1 P C P EA	4	C67528	Jul-81		
076	8 101-4822	1A RES 8.2K OHM 1/4W 5% R72	RP P 1 P C P EA	1	C67528	Jul-81		
057	8 101-4823	1A RES 82K OHM 1/4W 5% R46	RP P 1 C P EA	1	C67528	Jul-81		
048	8 108-1543	1A RES 1.54K OHM 1/4W 1% R84	RP P 1 C P EA	1	C75828	Jul-81		
042	8 108-1783	1A RES 1.78K OHM 1/4W 1% R10	RP P 1 C P EA	1	C75828	Jul-81		
041	8 108-1963	1A RES 1.96K OHM 1/4W 1% R105,104	RP P 1 * P EA	2	C75801	Mar-82		
047	8 108-3833	1A RES 3.83K OHM 1/4W 1% R93,R95-96,R97	RP P 1 * P EA	4	C75831	Jul-81		
039	8 108-3923	1A RES 3.92K OHM 1/4W 1% R65,66	RP P 1 P C P EA	2	C75828	Jul-81		
046	8 108-4531	1A RES 45.3 OHM 1/4W 1% R14	RP P 1 C P EA	1	C75828	Jul-81		
043	8 108-5623	1A RES 5.62K OHM 1/4W 1% R94,R98	RP P 1 C P EA	2	C75828	Jul-81		
106	8 109-0002	0 POT, TRIM 1K OHM 20%	RP P 1 P C P EA	1	442	10-Oct-83		
040	8 109-0005	A POT, TRIM 500 OHM, 20% ALTN F/N 109-0420	RP P 1 * P EA	1	C04518	May-82		
098	8 109-0410	1A POT, 500 OHM 18 - 25 TURNS	RP P 1 C P EA	1	C50428	Jul-81		
099	8 109-0420	MA POT, 1 TURN .250 DIA, 500 OHMS ALTN F/N FOR ITEM 40	RP P 1 C P EA	0	P10518	May-82		
038	8 111-0023	1A RES NETWORK 7 X 560 OHM 5% RF2-8	RP P 1 C P EA	7	C67528	Jul-81		
094	8 111-0024	1A RES NETWORK 7 X 4.7K OHM 5% RF-1	RP P 1 C P EA	1	C67528	Jul-81		
059	8 127-0100	1B CAP TANT 4.7 UF 20% 10V C59	RP P 1 * P EA	1	C59928	Jul-81		
037	8 127-0101	1B CAP TANT 10 UF 20% 15/16V C38-C40	RP P 1 * P EA	3	C59928	Jul-81		
029	8 130-0002	1B CAP CER AXIAL .01 UF +80%-20% 25V C1,2,6,7	RP P 1 P C P EA	4	C93928	Jul-81		
097	8 130-0003	1B CAP CER AXIAL .1 UF +80%-20% 25V C13,C14	RP P 1 P C P EA	2	C939		14-Apr-83	
028	8 140-0007	1B CAP CER AXIAL .1 UF +80%-20% 25V C3,5,10,16,21,22,25, C27,28,31,40,45,4	RP P 1 C P EA	31	C93901	Mar-82		
031	8 170-0200	1A CAP CER 100UF 10% 25V C29,35	RP P 1 C P EA	2	C56028	Jul-81		

EFFECTIVITY DATE: ALL J N D E N T E D B I L L S O F M A T E R I A L

PARENT PART: A3M305 7 PROFILE FOR W/FILE 777 UM: EA PROD CODE: 0H LCN: F354 ASSEMBLY QTY: 1  
REQ: B SERI CODE: G TYFF: J ABC: \* PLAN CODE: F DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	REMARKS	FR ST S A P CD C Y F B L U M	EXTENDED QTY PER	ECN CHG	START DATE	END DATE	S/N	CLOSE DATE	S/N
036	8 137-5401	1A CAP DIF MICA 20 PF 5% 500V		RP P 1 C P EA	1	C54128	Jul-81				
		C31									
035	8 137-5701	1A CAP DIF MICA 47 PF 5% 500V		RP P 1 F C P EA	1	C54128	Jul-81				
		C34									
034	8 137-5801	1A CAP DIF MICA 75 PF 5% 500V		RP P 1 C P EA	1	C54128	Jul-81				
		C8									
032	8 137-6101	1A CAP DIF MICA 100 PF 5% 500V		RP P 1 F C P EA	1	C54128	Jul-81				
		C33									
033	8 137-6301	1A CAP DIF MICA 150 PF 5% 500V		RP P 1 C P EA	4	C54128	Jul-81				
		C9, C18, C17, C20									
027	8 151-4701	1C INDUCTOR, 5.6 OHM 10% L1, L2		RP P 1 * P EA	2	C39528	Jul-81				
021	8 156-0100	A DELAY LINE 14 PIN DIF 100 OHM, 50 DLY 2		RP P 1 * P EA	1	792 28	Jul-81				
022	8 156-0110	A DELAY LINE 14 PIN DIF 500 OHM, 100 DLY 1		RP P 1 * P EA	1	792 28	Jul-81				
007	8 301-0045	A IC, 7445 U4		RI P 1 C P EA	1	C06328	Jul-81				
001	8 301-0074	A IC, 7474 U2		RI P 1 F C P EA	1	C06328	Jul-81				
005	8 305-0014	A IC, 74LS14 U30		RI P 1 P B P EA	1	442 28	Jul-81				
002	8 305-0174	A IC, 74LS174 U29		RI P 1 P B P EA	1	442 28	Jul-81				
004	8 307-0064	A IC, 74S64 U27		RI P 1 B P EA	1	C06328	Jul-81				
013	8 325-0102	A QUAD 2-INPUT NOR GATE U18		RI P 1 C P EA	1	741 28	Jul-81				
010	8 325-0107	A TRIPLE 2-INPUT EXCL OR/EXCL NOR GA U10, U15		RI P 1 C P EA	2	741 28	Jul-81				
008	8 325-0114	A TRIPLE LINE RECEIVER U5, U14		RI P 1 C P EA	2	741 28	Jul-81				
009	8 325-0116	A TRIPLE LINE RECEIVER U26, U9		FI P 1 C P EA	2	741 28	Jul-81				
012	8 325-0117	A DL 2-WID 2-3-INPT OR-AND/OR-AND-I U16		RI P 1 C P EA	1	741 28	Jul-81				
011	8 325-0131	B IC ECL HIGH SPEED DUAL D FLIP-FLO U11,17,19,20,21,22		RI P 1 C P EA	6	C25528	Jul-81				
006	8 327-0453	A IC, DUAL PERIPHERAL DRIVES U3		RI P 1 * P EA	1	757 28	Jul-81				
096	8 335-0007	A PROG HEX 16 INPT REG AND-OR GT		RI P 1 P B P EA	1	642 28	Jul-81				
003	8 341-0069	A MEMPAL		RL A 1 * P EA	1	P10501	Mar-82				
014	8 741-0002	A IC, 741-0002		RI P 1 C P EA	3	750 28	Jul-81				
016	8 741-0003	A IC, 741-0003		RI P 1 C P EA	1	750 28	Jul-81				

PROG HEX 16 INPT REG AND-OR GT AR RI P 1 P B P EA  
MEMPAL RL A 1 \* P EA  
MEM AND 06 01 00Y  
U30  
A IC, 741-0002 QUAD 2-INPUT GEN PURPOSE RP P 1 C P EA  
U21, U 1, U2  
A IC, 741-0003 QUAD 2-INPUT HIGH SPEED, RP P 1 C P EA

EFFECTIVITY DATE: ALL

INDEXED BILLS OF MATERIAL

PARENT PART: A3M0305  
 PARENT PART: A3M0305  
 ECN: F354 ASSEMBLY QTY: 1  
 DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	PR ST S A P CD C Y F B L U M	EXTENDED QTY PER	ECN CHG	START DATE	CLOSE DATE	S/N
050	8 353-0005	A IC REG, +5V 100MA TO 92, 3 TERMNL RI P 1 U1, U24 ITEM 100-102 ALT P/N	C P EA	1	792	28-Jul-81		
018	8 353-0319	A IC, HIGH SPEED DUAL COMPARATOR RG1	R I P 1 C P EA	1	750	28-Jul-81		
017	8 353-0353	A DUAL FET OF AMP/BUFFER U13	R P F 1 C P EA	2	750	28-Jul-81		
015	8 353-0592	A IC, VIDEO AMPLIFIER U25, U8	R I P 1 C P EA	1	750	28-Jul-81		
024	8 371-4152	1A DIODE FAST SWITCH 1N4152 500mW 30 U6 CR1-14, CR16-21,	R P P 1 C P EA	23	C53828	Jul-81		
100	8 372-2022	1A TRANS,NFN,SWITCHING AND AMP 2N222 CR23-24, CR26 ALT P/N FOR ITEM 23	* * * * EA	0	C40308	Jul-83		
101	8 372-2907	A XSTR,2N2907, PNF SWITCH & AMPLIFI U1-QTY 2 ALT P/N FOR ITEM 23	* * * * EA	0	C25908	Jul-83		
102	8 372-3904	A TRANSISTOR,NFN SW,8AMP, 2N3904 U1-QTY 2 ALT P/N FOR ITEM 23	R P P 1 P C P EA	0	C30308	Jul-83		
103	8 372-3906	1B TRANSISTOR,NFN SW,8AMP, 2N3906 U24-QTY 2 ALT P/N FOR ITEM 23	R P P 1 P C P EA	0	C76808	Jul-83		
026	8 375-0010	1A DIODE REFERENCE 10mA 1.2V U24-QTY 2	R P P 1 C P EA	1	C53828	Jul-81		
019	8 375-0012	1A DIODE DUAL VOLT VAR CAP 200mA 32V CR15	* P EA	1	C53828	Jul-81		
020	8 376-0016	A FET, N-CHANNEL VOLT CONTROL RESIS. 02 U1-QTY 1	R P P 1 * P EA	1	C30328	Jul-81		
090	8 511-0801	C SOCKET, IC 8 PIN 01	R P P 1 P C P EA	3	799	28-Jul-81	14-Apr-83	
091	8 511-1401	C SOCKET, IC 14 PIN	R P P 1 P C P EA	12	799	28-Jul-81	14-Apr-83	
092	8 511-1601	C SOCKET, IC 16 PIN	R P P 1 P C P EA	17	799	28-Jul-81	14-Apr-83	
093	8 511-2001	C SOCKET, IC 20 PIN	R P P 1 P C P EA	1	799	28-Jul-81	14-Apr-83	
089	8 515-0005	1B CONN,PIN,SINGLE	R P P 1 P C P EA	15	C78128	Jul-81		
087	8 515-0120	1A CONN,HDR,3GL ROW,4P	R P P 1 * P EA	1	C78128	Jul-81	02-Mar-82	
085	8 515-0130	1R CONN,HDR,FT ANG,DEL ROW,8/16P J5	R P P 1 * P EA	1	C78128	Jul-81		
088	8 515-0131	1R CONN,HDR,RT ANG,DEL ROW,17/34P J2	R P P 1 C P EA	1	C78101	Mar-82	28-Aug-83	
086	8 515-0140	1A CONN,HDR,RT ANG,5P,W/LKG RAMP J6-8	R P P 1 * P EA	3	C78128	Jul-81		
095	8 515-0160	1A CONN,HDR,RT ANG,DEL ROW,17/34P J5-8	* * * * EA	1	C78128	Jul-83		
104	8 515-0161	1E TURNING, HEAT SHIELD 1-A JB BLACK USE W/MT 10P 10W P/N FOR ITEM 104	E X 7 P C P FT	0	C50308	Jul-83		

EFFECTIVITY DATE: ALL

IDENTIFIED RILLS OF MATERIAL

PARENT PART: A3M0305  
REV: P  
TYPE: G  
UM: FA  
PROD CODE: DH  
ECN: F354  
ASSEMBLY QTY: 1  
DATE: 15-Mar-84

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	FR S T S A F U M	EXTENDED QTY PER	ECN	START DATE	CLOSE DATE	S/N	
006	4	1A DRESS PANEL, DRIVE, PROFILE	RM F 1 * P EA	1	F56714-Dec-82				
007	4	1B DRESS PANEL, PWR SPLY PROFILE	RM F 1 * P EA	1	F64414-Dec-82				
012	4	R LABEL, FCC NON COMPLT\$(RTKOH&HQ, 7 P C F EA	7 P C F EA	1	F59321-Mar-83				
002	3	1R MFG ASSY, ACC FAC, FG, PROFILE	** * * EA	1	F35414-Dec-82		01-Sep-83		
007	4	AB FORM, USER INPUT REPORT A3	EX X 7 P C F I						
B2 .J.									
5B	JXA5RJA4BH	1E REGIS. CARD, PERIF. & SOFTWARE	EX X 7 P C P EA	1	A92714-Dec-82		01-Sep-83		
009	4	1C MANUAL, USER'S, PROFILE FOR A3	EX P 7 C P EA	1	F63414-Dec-82		01-Sep-83		
005	4	1D UNPACKING INSTRUCTIONS, PROFILE	EX X 7 C P EA	1	F72914-Dec-82		01-Sep-83		
006	4	R PACKING LIST, PROFILE	EX X 7 * P EA	1	F31714-Dec-82		01-Sep-83		
016	4	A NOTICE, PROFILE	EX P 7 * P EA	1	F13814-Dec-82		01-Sep-83		
015	4	C PROFILE HELPFUL HINTS	EX X 7 * P EA	1	F17714-Dec-82		01-Sep-83		
002	4	1D CABLE, A.C. POWER CORD	2M F 1 P C P EA	1	A86214-Dec-82		01-Sep-83		
003	4	1E DISKETTE ASSY, A3 PROFILE DRIVER	WS A 1 C P EA	1	L27314-Dec-82		01-Sep-83		
001	5	1 DISKETTE, BLANK, WRITE PROTECTED	RD P 1 P C P EA	1	332 31-Aug-81		01-Sep-83		
002	5	1E LABEL, DISKWARE, A3 PROFILE DRIVE	EX X 7 * P EA	1	L15131-Aug-81		01-Sep-83		
000	5	C DISKETTE ASSY, SYSTEM UTILITIES	RD A 1 P C P EA	0	995 01-Mar-82				
004	6	1A NOT USED THIS ASSEMBLY	D * P D P EA	0	NONE				
001	6	1 DISKETTE, BLANK, WRITE PROTECTED	RD P 1 P C P EA	0	332 29-Jan-81				
001	6	C LABEL, DISKWARE SYSTEM UTILITIES	EX X 7 P C P EA	0	995 29-Jan-81				
002	6	C DWG, DISKWARE ASSY APPLE 3	EX D 7 * U EA	0	995				
003	6	B ENVELOPE, DISKETTE APPLE 3	EX X 7 P C P EA	1	568 29-Jan-81				
003	5	R ENVELOPE, DISKETTE APPLE 3	EX X 7 P C P EA	1	568 31-Aug-81				
004	4	3D DISKETTE ASSY, A3 PROFILE "DEMO"	WS A 1 C P EA	1	F57414-Dec-82		01-Sep-83		
001	5	1 DISKETTE, BLANK, WRITE PROTECTED	RD P 1 P C P EA	1	332 19-Oct-81				
002	5	1D LABEL, DISKWARE, A3, PROFILE DEMO	EX X 7 * P EA	1	F37819-Oct-81				
000	5	C DISKETTE ASSY, SYSTEM UTILITIES	RD A 1 P C P EA	0	995 19-Oct-81				
004	6	1A NOT USED THIS ASSEMBLY	D * P D P EA	0	NONE				
001	6	1 DISKETTE, BLANK, WRITE PROTECTED	RD P 1 P C P EA	0	332 29-Jan-81				
002	6	C LABEL, DISKWARE SYSTEM UTILITIES	EX X 7 P C P EA	0	995 29-Jan-81				
000	6	C DWG, DISKWARE ASSY APPLE 3	EX D 7 * U EA	0	995				
003	6	B ENVELOPE, DISKETTE APPLE 3	EX X 7 P C P EA	1	568 29-Jan-81				
003	5	R ENVELOPE, DISKETTE APPLE 3	EX X 7 P C P EA	1	568 31-Aug-81				
018	4	1C SURASSY, DSKW BACKUP /// A3	WS N 1 * P EA	1	L24103-Jan-83				
002	5	1A MANUAL, BACKUP III	EX P 7 * P EA	1	F59903-Jan-83		01-Sep-83		
001	5	R ASSY DISKETTE BACKUP III	WS A 1 * P EA	1	A41203-Jan-83				
004	6	1A NOT USED THIS ASSEMBLY	D * P D P EA	0	NONE15-Nov-82				
001	6	1 DISKETTE, BLANK, WRITE PROTECTED	RD P 1 P C P EA	1	332 15-Nov-82				
002	6	B LABEL, DISKWARE BACKUP /// A3	EX P 7 * P EA	1	A41228-Jan-83				
000	6	C DWG, DISKWARE ASSY APPLE 3	EX D 7 * U EA	0	995 15-Nov-82				
003	6	B ENVELOPE, DISKETTE APPLE 3	EX X 7 P C P EA	1	568 15-Nov-82				
000	6	1A MANUAL, BACKUP III	EX P 7 * P EA	1	F33703-Jan-83				
000	6	R ASSY DISKETTE BACKUP III	WS A 1 * P EA	1	A41203-Jan-83				
003	6	1A NOT USED THIS ASSEMBLY	D * P D P EA	0	NONE15-Nov-82				
001	6	1 DISKETTE, BLANK, WRITE PROTECTED	RD P 1 P C P EA	1	332 15-Nov-82				
002	6	B LABEL, DISKWARE BACKUP /// A3	EX P 7 * P EA	1	A41228-Jan-83				
000	6	C DWG, DISKWARE ASSY APPLE 3	EX D 7 * U EA	0	995 15-Nov-82				
003	6	B ENVELOPE, DISKETTE APPLE 3	EX X 7 P C P EA	1	568 15-Nov-82				
000	6	1A MANUAL, BACKUP III	EX P 7 * P EA	1	F33703-Jan-83				
000	6	R ASSY DISKETTE BACKUP III	WS A 1 * P EA	1	A41203-Jan-83				
003	6	1A NOT USED THIS ASSEMBLY	D * P D P EA	0	NONE15-Nov-82				
013	4	R LABEL, OPEN ME FIRST PROFILE	EX P 7 * P EA	1	L30901-Oct-83		01-Sep-83		
012	4	1B LABEL, APP FAC PROFILE FOR A3	EX P 7 * P EA	1	F42414-Dec-82		01-Sep-83		
014	4	1C LABEL, APP FAC PROFILE FOR A3	EX P 7 * P EA	1	F63914-Dec-82		01-Sep-83		
011	4	1D LABEL, APP FAC PROFILE FOR A3	EX P 7 * P EA	1	F32914-Dec-82		01-Sep-83		



EFFECTIVITY DATE: ALL

INDIVIDUAL BILLS OF MATERIAL

PARENT PART: 03M0305

3 PROFILE FOR APPLE ///

UM: FA PROD CODE: DH

ECN: F354 ASSEMBLY QTY: 1

ERC: B SRCE CODE: G TYPE: 1

ABC: \* PLAN CODE: P

DATE: 15-Mar-83

ITEM LEVEL	COMPONENT PART NUMBER	E PART DESCRIPTION	REMARKS	PR ST S A P	CD C Y F B L U M	EXTENDED QTY PFR	ECN CHG	START DATE	S/N	CLOSE DATE	S/N
020 3	825-0114	1E LABEL, PROFILE MODEL & SERIAL NO.		EX P 7	* P EA	1	F63114	Dec-82		01-Sep-83	
007 3	825-0116	C LABEL, INDIVIDUAL CARTON PROFILE		EX P 7	* P EA	1	F28414	Dec-82		01-Sep-83	
010 3	825-0207	B LABEL, FCC NON COMPLIANCE APPLE 3		EX X 7	P C P EA	1	F59314	Dec-82		01-Sep-83	
024 3	825-0311	1R LABEL, LOGO 16MM BY 16MM		EX X 7	P C P EA	1	F51415	Feb-83		01-Sep-83	
025 3	825-0313	1R LABEL, NAMEPLATE, PROFILE		EX P 7	* P EA	1	F51415	Feb-83		01-Sep-83	
026 3	825-0315	1C LABEL, LED PROFILE		EX P 7	* P EA	1	F51415	Feb-83		01-Sep-83	
009 3	825-0317	A LABEL, FRAGILE, PROFILE		EX P 7	* P EA	4	F11214	Dec-82		01-Sep-83	
013 3	825-0328	A LABEL, DO NOT REMOVE END CAPS		EX P 7	* P EA	1	F12514	Dec-82		01-Sep-83	
014 3	825-0329	A LABEL, SERIAL NUMBER		EX P 7	* P EA	0.6000	F12414	Dec-82		01-Sep-83	
016 3	918-0050	R ANGLE BOARD, FALLETTIZING, 2X2X36		EX X 7	S C U EA	0.3330	M58314	Dec-82		01-Sep-83	
017 3	918-0051	R SEALS, STRAPPING, 50 DY		EX X 7	S C P EA	0.3330	M58314	Dec-82		01-Sep-83	
018 3	918-0052	R TAPE, STRAPPING, CONTRAX 816		EX X 7	S A P EA	0.0007	M58314	Dec-82		01-Sep-83	
019 3	918-0071	R PALLET, 48 X 40 2 WAY ENTRY		EX P 7	B P EA	0.1670	M72514	Dec-82		01-Sep-83	
015 3	919-0010	A LABEL, MODEL TYPE "US STD"		* *	* * EA	1.3330	F33014	Dec-82		01-Sep-83	
			RUBBER STAMP OR PEN								
003 3	942-0117	1C BOX, 29.5 X 21.25 X 16.13, PROFIL		EX X 7	C P EA	1	F39914	Dec-82		01-Sep-83	
011 3	942-0142	A BOX, OPF 19.25 X 10.75 X 6.88		EX P 7	* P EA	1	F12514	Dec-82		01-Sep-83	
022 3	946-0003	B TAPE, P.S. 2 inch X 60 yard		EX X 7	P C P RL	0	C06414	Dec-82		01-Sep-83	
			ALTN P/N FOR ITEM 8								
			ALTN QTY .059								
008 3	946-0008	A TAPE, SEALING GLASS WEB #341 A3		EX X 7	P B P RL	0.0150	474 14	Dec-82		01-Sep-83	
			ALTN P/N 946-0003								
			ALTN P/N 946-0011								
023 3	946-0011	A TAPE, PRESSURE SENSITIVE 2 INCH, AU		EX X 7	* P RL	0	C04914	Dec-82		01-Sep-83	
			ALTN P/N FOR ITEM 8								
			ALTN QTY .0035								
006 3	946-0012	1C STRAPPING, POLYPRO 1/2 INCH		EX X 7	* P RL	0.0010	F72214	Dec-82		01-Sep-83	